# ALTERNATIVE LITHOGRAPHY STRATEGIES for FLEXIBLE ELECTRONICS

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# ALTERNATIVE LITHOGRAPHY STRATEGIES FOR FLEXIBLE ELECTRONICS

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## Chapter 1

# General Introduction

Flexible electronics is an area of research and development that foresees the fabrication of faster, lighter, thinner, bendable and cheaper devices manufactured on low-cost polymeric foils. Classical and new patterning strategies for high-throughput, large-volume roll-to-roll (or reel-to-reel) manufacturing lines, which are known from newspaper printers, are being developed to further reduce manufacturing costs. Examples of inventions and products soon to hit the market are flexible organic light-emitting diode- (OLED-)based displays,[1-3] radio-frequency identification (RFID) tags,[4, 5] and organic solar cells (OSCs).[6-8]

Renowned patterning techniques face new challenges when patterning high-resolution flexible electronics, not necessarily originating from the small dimensions of the device, but from deformations and the dimensional instability of the polymeric foils. Reversibly gluing of the foil onto a carrier (foil-on-carrier; FOC) improves the mechanical and in-plane stability during processing. As a low-cost patterning technique with routine nanometer patterning capabilities, nanoimprint lithography (NIL) has been identified as one of the ten next-generation lithography techniques to manufacture high-density integrated circuits and optics. The capability of NIL to pattern complex electronic devices on flexible substrates is studied in this thesis (Chapters 3-5). Flexible thin-film transistor demonstrators are patterned on poly(ethylene naphthalate) (PEN) foil by UV NIL, and their electrical performance is determined.

A restriction to the patterning process and materials introduced by the cheap polymeric foils, is the limitation of the temperature window to around 150°C.[9] The low glass transition temperature of the polymeric foils

(e.g. ~70-85°C for PET[10]) requires alternative deposition techniques and newly engineered materials. Especially high-*k* dielectrics and highly conductive, metallic structures need to be deposited and patterned on polymeric foils. The sintering behavior and resulting conductivity of metallic precursor inks are often studied for inkjet-printed features. Alternative lithographic processes to fabricate metallic, conductive structures from metallic precursor materials are presented in Chapters 6 and 7, which simultaneously allow the directed deposition of materials in channels without alignment. Currently, the reported top-down methods aim to make self-aligned TFTs by smartly masking the different layers of the electronic device.[11-14] The processes studied here can be a first step towards a solution-based, self-aligned TFT.

The historical development of the first mass-printing strategies to high-resolution, alternative patterning techniques is reviewed in Chapter 2. Its main focus is on large-area patterning of flexible electronics. Patterning techniques are compared, and their individual benefits and limitations discussed. The three most promising soft lithographic techniques in large-area printing, and the family of NIL, are described from the viewpoint of flexible electronics.

A novel thermal imprint process on Si and foil is presented in Chapter 3, capable of imprinting structures simultaneously from the submicron to the millimeter scale. With the new thermal imprint process, many resist combinations can be employed for tailored nanofabrication. In the example given, two resists with different etch resistivities are combined, allowing the complete removal of an inhomogeneous residual layer on foil.

In Chapter 4, the source-drain layer of a flexible TFT demonstrator is patterned by UV NIL. A thin and relatively homogeneous residual layer thickness is obtained with a newly developed FOC system, obtained by hot embossing. The electrical performance is compared to state-of-the-art photolithographically fabricated flexible TFTs.

All three layers of a flexible TFT demonstrator, presented in Chapter 5, are patterned with UV NIL in a multistep imprinting process. The waviness of the FOC is further reduced by introduction of a novel, step-and-flash imprinted planarization layer. The residual layer thickness and distribution is thereby reduced. Flexible TFTs with channel lengths from 5 µm down to 250 nm are presented and their electrical performance is discussed.

The filling mechanism of solutes in open microchannels formed by embossing of an epoxy resist on PET foil is studied in Chapter 6. The channel width-dependent filling and drying behavior is visualized by adding a fluorescent dye as the solute. Selective deposition of metallic precursor materials in the open microchannels is used to grow copper microwires from solution.

The soft lithographic patterning behavior of room temperature-sintering poly(acrylic acid)-capped silver nanoparticle dispersions is studied in Chapter 7. Silver wires are patterned on PET foil by micromolding in capillaries (MIMIC), and embedded silver wires are fabricated by selective filling of open microchannels. The sintering behavior and depth induced by two different sources of the particle-destabilizing chloride, and the resulting conductivity relative to bulk silver is studied. As an alternative printing technique, micron-sized Ag dots are repetitively printed with a hydrogel stamping system on an elastomeric substrate. The height and shape distribution of the printed silver dots, and the origin of defects is discussed. The thesis is concluded by a summary and outlook, in which future prospects of this work in the field of flexible electronics are discussed.

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## Chapter 2

# High-Resolution Patterning Strategies for Flexible Electronics

*In this chapter, the development of conventional mass-printing strategies into high-resolution, alternative patterning techniques is reviewed with a focus on large-area patterning on flexible substrates. In the first part, conventional and digital printing techniques are introduced and categorized. The limitations of conventional printing guides the reader to the second part of the review, describing alternative lithographic strategies for patterning on flexible foils for the fabrication of flexible electronics. Soft and nanoimprint lithography-based patterning techniques and their limitations are surveyed with respect to patterning devices on flexible foils. These device structures show a shift from fabricating simple microlense structures to more complicated, high-resolution electronic devices. The development of alternative, low-temperature processable materials and the introduction of high-resolution patterning strategies will lead to the low-cost, self-aligned fabrication of flexible displays and solar cells from cheaper but better performing organic materials.*

## 2.1 Introduction

With the invention of the first European movable type printing around 1440 by the goldsmith Johannes Gensfleisch zum Gutenberg, economical and multiple production of alphabet communication became feasible.[1] Knowledge spread rapidly and literacy increased as a result of typography. One of the first books widely spread across Europe was the Gutenberg Bible around 1450. Today, practically all movable type printing ultimately derives from Gutenberg's movable type printing, which is often regarded as the most important invention of the second millennium. Four conventional printing techniques exist, named after the type of master used for printing: relief printing (flexographic), intaglio printing (gravure), planographic printing (offset), and print through (screen printing) (Figure 2.1a-d).[2] Next to the conventional printing techniques, also two digital printing types are shown: inkjet printing and laser ablation (Figure 2.1e-f).

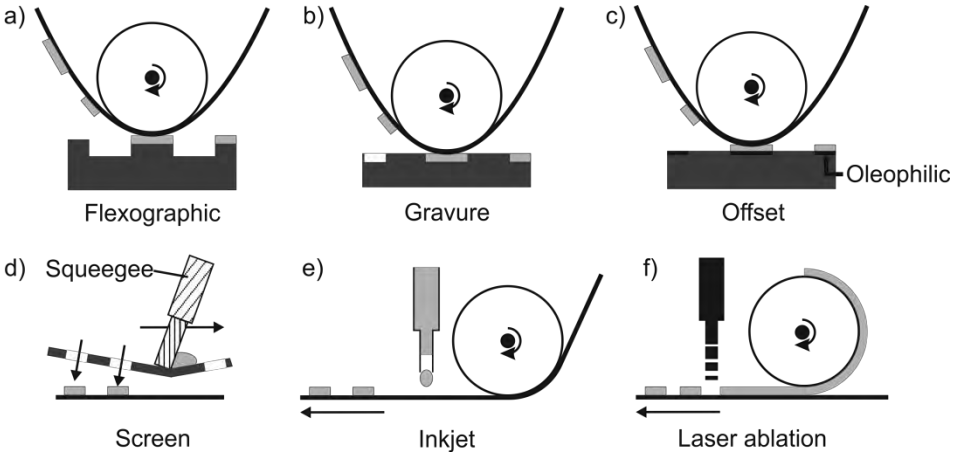


**Figure 2.1** Schematic illustration of four conventional and two digital printing techniques. The techniques can be categorized into (a-d) impact and (e-f) non-impact printing, and furthermore in (a-e) additive and (f) subtractive patterning. Illustrations are based on [2].

In flexographic printing, the ink is transferred from the protruding elements of the printing master to the substrate. In gravure printing the opposite occurs: the relatively low viscous ink is transferred from the pits of the master to the substrate. In offset, images are formed by the physicochemical difference between oleophobic and oleophilic areas on the

printing master, thus eliminating the need for a pattern relief. In screen printing, the color is pressed though a mesh onto the substrate. All four conventional printing techniques apply pressure to the substrate during ink transfer. In digital printing forms such as inkjet and aerosol jet (Figure 2.1e), a pattern is made from a digital image without applying pressure to the substrate. It is thus a non-impact technique. The ink is dropped from a nozzle onto the substrate. In the presented printing techniques, ink is deposited onto the substrate. Laser ablation (Figure 2.1f) however, is a subtractive patterning technique. With lasers, thin layers of a donor material can also be transferred, in a process called laser-induced forward transfer (LIFT), from a glass support onto an acceptor substrate (e.g. Si, foil) which is placed in close vicinity. In this process, developed by Bohandy[3] in 1986, a pulsed laser beam heats and melts for example a metal through the glass support. Upon sufficient heating, mainly glass components[4] are turned into their gaseous state at the glass/metal interface, building up high pressures that blast metal off the glass support. Metals,[3-5] liquids,[6-7] and organic materials[5, 8] have been transferred onto acceptor substrates with a highest resolution of 30 μm[5] to fabricate OTFTs on Si,[5] and polymer light-emitting diodes (PLEDs) on glass.[8] Flexible OLEDs and OFETs have been reported with a slightly altered LIFT process.[9] Direct laser damage of sensitive materials, such as organic dyes or semiconductive polymers, can be avoided by addition of a dynamic release layer (DLR), converting light to heat by thermal evaporation or chemical decomposition.[8] The absence of a printing master makes digital printing (incl. LIFT) more customizable and results in less waste with respect to chemicals and target material. Utilization of a digital master has the considerable advantage of reduced cost, as the cost and complexity of producing a master range from relatively low cost in the case of screen printing to medium cost for flexographic printing and very high cost for gravure printing.[10]

The area of printing continued to develop and expand from printed text on paper to printed electronics on other materials such as textiles and polymeric foils. Semiconductor research and the invention of the point-

contact transistor at Bell laboratories in 1947[11] by Bardeen, Brattain and Shockley was followed up by the invention of the first silicon transistor[12] by Texas Instruments in 1954 and the first metal-oxide-semiconductor field-effect transistor (MOSFET)[13] in 1960 again at Bell labs, paving the way to practically all modern electronics. The worlds ever demanding decrease of feature sizes for the fabrication of more densely packed, faster electronic circuits and devices has been described by Gordon Moore in 1965.[14] His law predicts the doubling of the number of transistors that can be placed inexpensively on an integrated circuit approximately every two years. Research and development of tools, allowing reproducible patterning at an ever decreasing scale, are in the focus of the semiconductor manufacturers. Fabrication costs and addition of device functionalities follow thereby Moore's law as a target roadmap. Since all competitors work with the identical development timeline, Moore's law can be viewed as a self-fulfilling prophecy.[15] However, the 2011 annual report of the International Technology Roadmap for Semiconductors maintained the in 2010 predicted slowing growth at the end of 2013,[16] after which time transistor counts and densities are to double only every three years. High-end products with extremely short switching times and high integration densities are made of conventional electronics, fabricated on small areas on rigid substrates with sophisticated, high energy consuming techniques.

More recently, the area of printed electronics encountered a rapid development towards flexible devices. The motivation for this development can be found in the promise of low-cost, high-volume, high-throughput production in roll-to-roll (R2R) or sheet-to-sheet (S2S) processing lines of electronic components or devices which are light weight and small, thin and flexible, inexpensive and disposable.[17] Typically, the aim is to fabricate (semi-) transparent, bendable and even rollable flexible electronic devices such as organic light-emitting diode (OLED)-based displays (Figure 2.2),[18] radio frequency identification (RFID) tags,[19, 20] and organic solar cells (OSCs).[21]

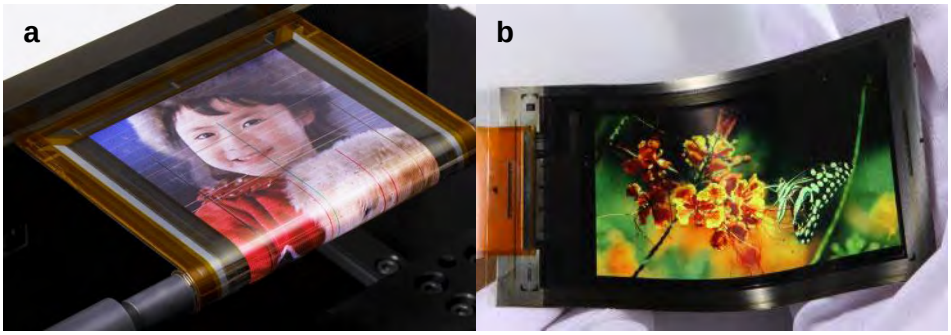


**Figure 2.2** Photographs of rollable AMOLED displays. (a) 4.1 inch OTFT-driven flexible OLED with a total thickness of 80 µm, presented by Sony at the SID-2010 in Washington, USA [22]. Reproduced with permission by the Society for Information Display. (b) 3.4 inch flexible AMOLED Display with 326 pixels per inch and a total thickness of 50 µm [23]. Copyright © 2011, The Japan Society of Applied Physics.

A key requirement for flexible displays and flexible complementary metal-oxide-semiconductor (CMOS) devices is the low temperature fabrication of organic thin-film transistors (OTFTs) on flexible substrates.[24] Flexible electronics face new challenges, not necessarily originating from the small dimensions of the device, but from the deformations and dimensional instability of the substrate.[25]

In the first part of this chapter, the history of mass-printing techniques is reviewed and examples of these printing strategies for the fabrication of flexible electronics are given and discussed. The next part describes the development of photolithography and the bottlenecks of processing on low-cost polymeric substrates. From the class of alternative high-resolution patterning strategies, soft and nanoimprint lithography are introduced and their applicability for the fabrication of flexible electronics discussed and reviewed.

## 2.2 Conventional Mass-Printing Techniques

### 2.2.1 Flexographic Printing

Flexographic printing (Figure 2.3) is a relief printing technique very similar to letterpress. The image is printed from protruding elements on a plate cylinder, transferring the image to almost any type of substrate including plastic, metallic films, cellophane, and paper. The elastic printing plate is made by exposure of a light-sensitive polymer, by computer-guided laser engraving, or through a molding process from a metallic plate creating a 3D relief in a rubber or polymer material. Every color has its own printing plate. Therefore, a multicolor picture requires mounting marks to ensure an exact build-up of the different elements of the picture. As mounting marks, microdots (down to 0.3 mm) and/or mounting crosses are utilized. Ink is transferred from the ink or fountain roll to an anilox roll, the textures of which hold a specific amount of ink. The amount of ink is controlled by the number of engraved cells (mostly inverted pyramids), ensuring an evenly and quick transfer of a controlled amount of ink with a uniform thickness to the printing plate. The anilox roll is typically made of chrome-coated ceramics or stainless steel, and represents the most sensitive part of the flexographic process. The amount of transferred ink critically depends on the quality of the cells. Wear of these cells results in less ink transfer or blurred images. Any excess of ink is removed from the anilox roll by a doctor blade. The reliefs on the printing cylinder pick out ink from the anilox roll (Figure 2.4), whereafter the ink is finally printed by pressing the web substrate against an impression cylinder.

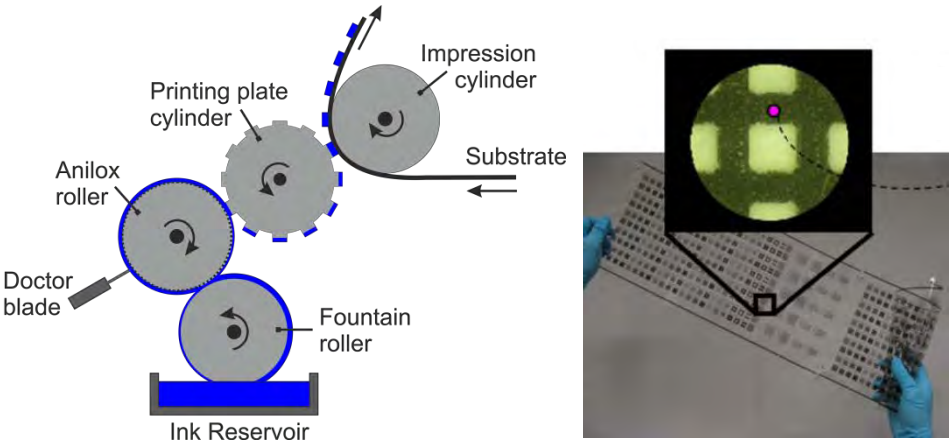


**Figure 2.3** Schematic illustration of flexographic printing, and a photograph of a flexographically printed sacrificial black ink on PEN foil [26]. Copyright © 2010 IEEE.

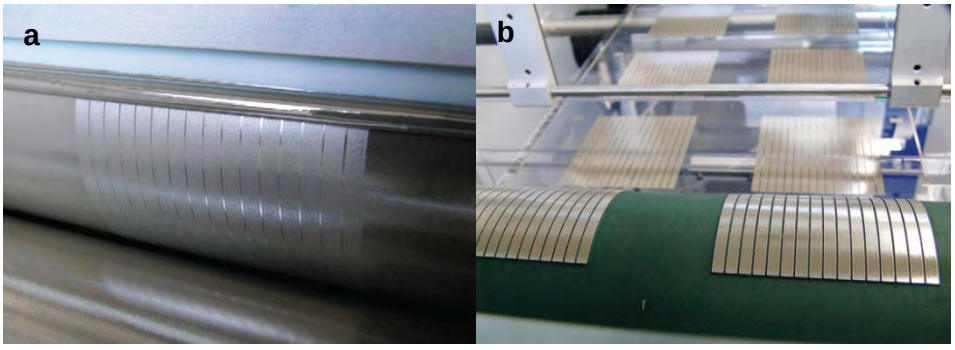


**Figure 2.4** Photograph of (a) an anilox roller after ink pick out from the printing cylinder. (b) The printing cylinder with a silver paste-inked relief during printing. The final printed pattern on the foil can be observed in the background. Reprinted from [27], Copyright © 2012, with permission from Elsevier.

Three line-ups of flexographic printing are known. In *stack press*, the color stations are stacked up vertically, allowing easy access and printing on both sides of the substrate. A good registration is obtained in *common impression press*, allocating all color stations in a circle around the impression cylinder. With *in-line press* heavier substrates, such as corrugated boards, can be printed by horizontally placed color stations. Next to the wide variety of substrates, a typical advantage of flexography is the wide range of inks that can be printed: solvent-based inks, water-based inks, electron-beam curing inks, UV curing inks and two-part chemically-curing inks (usually based on polyurethane isocyanate reactions).

With flexography, continuous conductive grids of Ag ink have been reported on indium tin oxide (ITO)-coated poly(ethylene terephthalate) (PET) foil with a minimal line width of 75 μm.[28] The typical resolution limit of 50-100 μm[29] for flexography can be reduced to ~20 μm by controlled edge dewetting and film breakup of inks, transferring for example Ag ink from a poly(dimethyl siloxane) (PDMS) mold to SU8-coated substrates.[30] In combination with slot-die coating, n-octanol has been flexographically printed on poly(3-hexylthiophene) : phenyl-C61-butyric acid methyl ester (P3HT:PCBM) to enhance the wettability for the following slot-die coated poly(3,4-ethylenedioxythiophene) - poly(styrene sulfonate) (PEDOT-PSS) layer for the fabrication of a polymer solar cell on PET foil.[10] With flexography, the dielectric and gate of a top-gate OTFT on PET foil have been printed, being the only mass-printing technique applying a sufficiently low pressure in order to avoid destruction of the underlying layers.[31] A lift-off process was introduced for the fabrication of the lower electrode of a microelectromechanical system (MEMS)-controlled Fabry-Perot display on poly(ethylene naphthalate) (PEN) foil, patterning a 2 μm thin sacrificial layer of black ink by flexography at 5 m/min (Figure 2.3).[26, 32]

Flexographic printing is designed for thin, uniform layers providing a better pattern integrity and sharper pattern edges than gravure printing.[26] It is characterized by a continuous reproduction of images or patterns on basically all types of substrates, including flexible foils and corrugated boards. Flexographic printing is less destructive than other mass-printing techniques, applying only low pressures to pre-patterned structures on the substrate.[31] In flexography, the formation of continuous, arbitrarily oriented, uniform lines does not rely on merging of discrete dots, which is different for screen, gravure and inkjet printing. The lack of a continuous line in the other three printing techniques, particularly for fine features, has a negative effect on the line consistency, caused by defects such as pin-holes, blocked cells and missing dots.[28] Flexographic printing of a liquid-phase ink material is prone to film instability and dewetting, thereby forming many defects such as open lines.[30] With flexography, only thin

layers can be printed, while gravure printing allows control over the feature thickness by adjusting the cell depth.

### 2.2.2 Gravure Printing

In gravure (intaglio) printing, an engraved cylinder is rolled over a moving substrate, typically paper or plastic (Figure 2.5).[33] Excess of ink is removed from the protruding elements of the cylinder by a doctor blade before the relatively low-viscosity ink is transferred from the cells to the substrate. Typical cell densities are between 220 and 400 cells per inch, with a groove or cell depth ~40 µm and width <100 µm.[34]

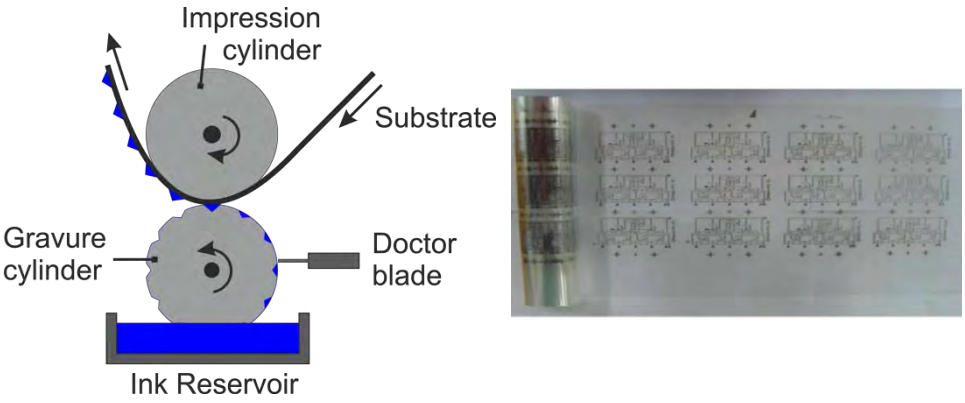


**Figure 2.5** Schematic illustration of gravure printing, and a photograph of R2R-gravure printed Ag-ink on PET [35]. Copyright © 2010 IEEE.

In daily life, rotogravure printed products can be found in the form of magazines, catalogues, packaging, decorative papers, etc. The width and thickness of printed dots depend on the cell emptying[34, 36] and drop spreading behavior, being a function of the depth and width of the engravings in the mold,[37] print speed, ink viscosity and the ink/substrate surface energies.[33] Uniform lines can be formed by merging droplets at a cell spacing to cell width ratio of 1.06 up to 1.40. At a ratio larger than 1.40, scalloped lines will be produced. Downscaling is believed to be possible with adjusted ink formulations. A study on overlay printing registration accuracy[35] showed a deficiency of 40 µm with a maximum of 59 µm parallel to the web moving direction and 16 µm with a maximum of 29 µm

in the perpendicular direction. The main reason for the attained large value is given by the variability in the web tension, vibration and thermal expansion of the gravure machine, and the thermal expansion of the PET substrate by Ag sintering at <150°C. A combination of rotogravure and inkjet printing has been utilized to fabricate top and bottom gate TFTs on PEN foil.[38] Gravure printing was used to print 70 nm thick, 20-21 µm wide Ag lines (rms roughness 5.8 nm), a 100 nm thin dielectric and the semiconductor. The top electrode was patterned by inkjet printing for precise alignment with a novel fluid guiding technique, resulting in an overlap with the gate and <20 µm line spacing. All-gravure printed OTFTs on PET foil with single-walled carbon nanotubes (SWNT) as a semiconducting layer have been reported, studying the overlay printing registration accuracy (OPRA) and line edge roughness of the source-drain electrodes.[39] Bottom-gate TFTs with a channel length of 170 µm, a width of 3000 µm, a thickness of 680 nm, OPRA of ±10 µm, and a surface roughness of 200 nm have been obtained. Gravure printing has also been used to pattern $SiO_2$ isolation and spacer structures of a MEMS-controlled display on PEN foil[26] and the semiconductor and dielectric of a ring oscillator on PET foil.[40] An optimized gravure plate design, containing the mesh, cell size, cell density, cell depth and cell angle was used to control the thickness of the $SiO_2$ to print three primary colors red, green and blue.

In summary, gravure printing is a mechanically simple process with fewer controlling variables when compared to competing high-speed printing processes such as flexography or offset lithography. It is known to be advantageous for its high-throughput, high-quality printing of half-tone images, and printability on different materials.[41] Gravure-printed layers are adjustable by the cylinder's cup design[26] (e.g. depth of cell), allowing thick layers to be printed on flexible substrates. Gravure printing requires a precise adjustment of each ink formulation regarding its viscosity and surface energy,[42] allowing also printing of low viscosity inks (e.g. semiconductor inks)[31] which cannot be handled by the other mass printing techniques. Furthermore, the fabrication of the gravure plate is more expensive compared to other printing techniques.[10]

### 2.2.3 Offset Printing

In offset lithography (Figure 2.1c), introduced at the end of the 18th century by Alois Senefelder,[2] images are formed by the physicochemical difference between oleophobic and oleophilic areas on the printing master, thus not requiring a pattern relief. The main carrier is oleophobic and often made of aluminum, while the color is taken up mostly by an oleophilic grease layer. Offset-printed features have typically a resolution in the range of 20 µm and a layer thickness below 1 µm,[43] allowing microstructuring up to 200 000 $m^2$/h. Offset-printed top gate TFTs have been reported on PET foil, showing a gap width in the range of 50 µm and a linewidth down to 100 µm. The dry layer thickness obtained for printed PEDOT was 600 nm.[43]

A modified offset printing technique[44] (Figure 2.6) has been developed by LG Display Co., printing thin and uniform layers of etch resist to form fine patterns of 10 µm width and 6 µm spacing as short channels of a TFT on Si. In the modification, an ink-coated roll blanket with low surface energy is pressed against a patterned printing plate (Figure 2.6) with high surface energy. Undesired ink is transferred to the printing plate, leaving the desired patterns on the roll blanket. The patterns are printed in the subsequent step from the blanket onto the substrate by rolling.

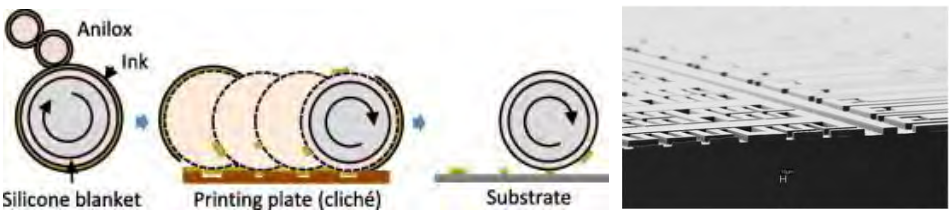


**Figure 2.6** Schematic illustration of modified offset printing and scanning electron microscopy image of the Si printing plate. Reprinted from [44], Copyright © 2012, with permission from Elsevier.

Offset printing is, in summary, an attractive patterning strategy for the source and drain patterning of top-gate OTFTs. The printing plate fabrication is comparatively simple and inexpensive.[31] At the same time it shares the high resolution and layer quality of gravure printing. On the

other hand, the layer thickness resulting from offset-printed features is reported to be more inhomogeneous showing a higher surface and edge roughness when compared to other mass-printing techniques. In a given example,[31] the average layer thickness was 600 nm with observed local layer thicknesses from 50 nm to 3 µm on PET foil.

### 2.2.4 Screen Printing

In screen printing,[45] ink is pressed with a squeegee through a screen onto the substrate. The screen is made of a porous mesh, from materials such as a porous fabric or stainless steel, stretched tightly over a frame made of wood or metal. Proper tension is essential for accurate color registration. The image to be replicated, the stencil, can be photochemically or manually defined on the mesh. The squeegee is typically made of a rubber, and is therefore prone to wear. Due to the simplicity of the process, a wide variety of substrates and inks can be used, allowing a high layer thickness which is typical for screen printing. From the three types of screen printing, *rotary screen printing* (Figure 2.7b, d) has the highest throughput, edge definition/ resolution and achievable wet thickness.[27] In the other two techniques, *flat-bed* (Figure 2.7a, c) and *cylinder*, a flat screen is pressed against a substrate. In flat-bed, the substrate is positioned horizontally parallel to the screen, while in cylinder press the substrate is mounted on a cylinder. Screens for rotary screen printing are seamless thin metal cylinders. The squeegee in rotary screen printing is fixed in the cylinder (Figure 2.7b),[27] or it is a free floating steel bar inside the cylinder with a magnetic pressure control.[45] Rotary screen presses are most often used for printing textiles, wallpaper, and other products requiring seamless continuous patterns.

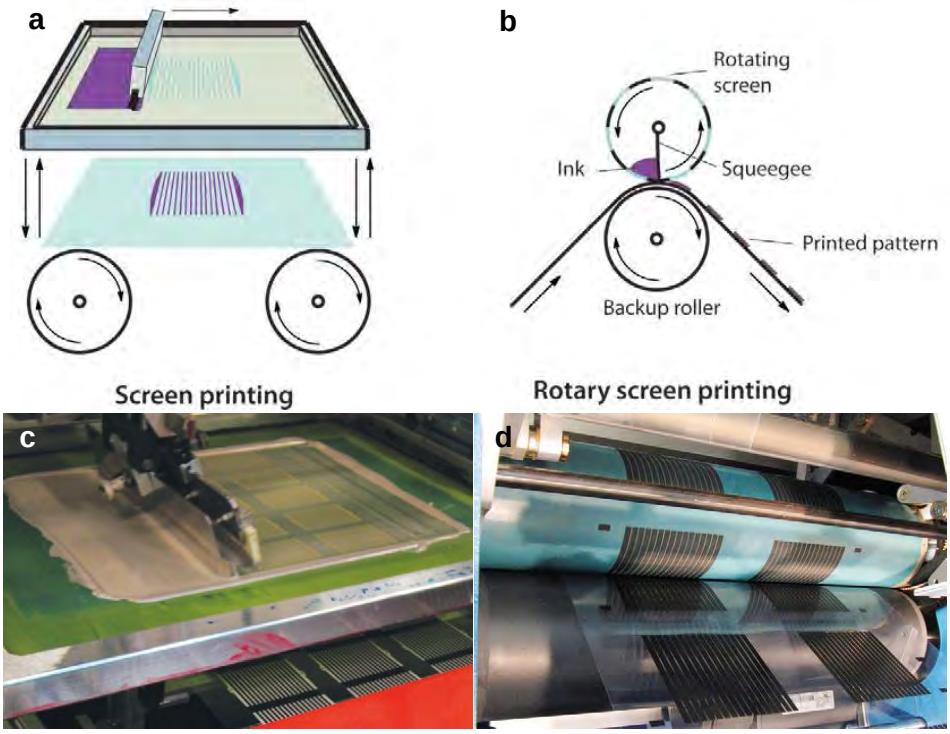


**Figure 2.7** Schematic illustration and photograph of (a, c) flat-bed and (b, d) rotary screen printing. (c) Flat-bed screen printing of silver paste showing how the squeegee forces the ink through the screen onto the underlying foil. (d) Rotary screen printing of conducting graphite ink onto a clear polyester foil. Reprinted from [27], Copyright © 2012, with permission from Elsevier.

In industrial processes, screen-printed films usually have a thickness larger than ~0.5 µm.[46] Thin and homogeneous layers are not easily obtained by screen printing. As an example, the inhomogeneous 100 nm hole transport layer of an OLED has been reported.[47] Nevertheless, also a 40 nm thin active layer of a bulk hetero-junction photovoltaic device with an rms value of 2.6 nm has been reported.[46] Both devices have been fabricated on glass substrates. Silk screen-printed polymer solar cells have been reported on PET foil by Krebs et al..[48] The anode pattern was defined into an ITO-coated PET foil by rotary screen printing an etch resist and subsequent etching. Electrical contacts made of epoxy silver paste and the conjugated polymer were also screen printed. A screen with a thread diameter of 27 µm and a mesh count in the range of 140-220 $cm^{-1}$ was used. Flexible

pentacene transistors have been demonstrated[49] with room temperature, silk screen printed silver resist, forming the top contact source-drain electrodes on poly(phthalate carbonate) foil. The channel length was varied from 40 μm to 200 μm at a fixed channel width of 1.5 mm. CMOS devices on PEN foil[50] have been fabricated by laser ablation of a 30 nm gold source-drain layer and screen printing. The p- and n-type semiconductor, a 800 nm-thick dielectric fluoropolymer and a gate layer of silver paste were subsequently screen printed, showing a process alignment of ± 25 μm for all printed materials. With the printed inverters, a voltage-controlled oscillator and two differential organic amplifiers were presented. Very recently, a solely screen-printed device, a flexible thin film supercapacitor on polyester (PE) foil, has been reported.[51]

Screen printing is an inexpensive, large-area printing technique with good control over the deposition area. This is important, for instance, for fabricating a device that is integrated onto a substrate containing other electronic devices. The quality of screen-printed films depends highly on: the number of fibers in the screen mesh, the tension of the mask, the distance from the mask to the substrate, the characteristics (hardness, edge) and process parameters (speed, pressure, angle) of the squeegee, the temperature, the humidity and the air flow around the printing area.[52] The ink viscosity is linked to all parameters mentioned, and has to be critically adjusted to match the mesh used in the screen mask such that the polymer solution will not run through the mask but will be transferred through the mesh upon application of mechanical pressure.[48]

### 2.2.5 Inkjet Printing

A printing technique in the field of organic, large-area electronics often combined with the above reviewed mass-printing techniques is the additive, direct patterning technique of inkjet printing. Therefore, it will be discussed in this section. Precise quantities of a wide range of materials can be deposited in the form of conducting lines or single droplets on various substrates (e.g. foils). It is a low-cost, non-impact and rapid technique with

a large potential to manufacture electronic circuits. Costs are reduced owing to digital imaging, eliminating the multiple process steps involved in using a photolithographically defined etch mask and the subsequent deposition and etching steps. As inkjet printing is a relatively fast technique, it potentially enables fast R2R patterning of conductive precursor materials,[53] such as metal nanoparticles[54, 55] or metal–organic complexes.[56]

The key challenge is developing suitable ink formulations, determining the drop ejection characteristics and dictating the quality of the printed electrocircuits by influencing the evaporation behavior and orientation (e.g. crystal orientation) upon solvent evaporation. Clogging of nozzles is a serious issue of inkjet printing and can reduce the yield substantially. The resolution is limited to 20 to 50 μm by statistical variations of the flight direction of droplets and their spreading on the substrate.[57] Especially in metal conductive inks, uniform and monodisperse metal nanoparticles in aqueous or organic solvent dispersions[58] contribute to attain a high dispersion stability and low electrical resistivity at low metallization temperatures.[54] The typical sintering step needed to render the precursor compound conductive, requires >30 min process time and/or higher temperatures (>250°C).[53] High sintering temperatures are incompatible with common polymer foils, such as PET and polycarbonate (PC), having a relatively low glass transition temperature. The choice of foil is therefore restricted to more expensive polymers such as polyimides (PI).[53]

Among the inkjet-printed metal conductive inks, Ag formulations receive a lot of attention,[58] and the first Ag inks are commercially available (e.g. BayInk® nanoparticulate silver inks, *Bayer Material Science*). A second type of Ag ink is known as a metal-organic decomposition (MOD) ink. Typically, heat is required to precipitate the metal and burn off the organic ligand in MOD inks, or, in case of NP inks, decompose the organic stabilizer.[53] Reported room temperature sintering techniques destabilize the metal inks by slow evaporation of the solvent or in a faster approach by chemical destabilization. As an example, the coalescence of Ag NPs by exposure to

HCl vapor has been reported (see also Chapter 7 in this thesis).[58, 59] Inkjet printing of seeding particles for subsequent electroless deposition of metals is another R2R-compatible route to metal lines.[60] Inkjet-printed, conjugated polymers have been reported in LEDs and, in combination with photolithographic patterning of hydrophilic and hydrophobic areas, TFTs on glass.[57] Fully inkjet-printed TFTs have been reported that were fabricated through patterning and sintering each individual layer of the device at an annealing temperature <150°C (compatible to PET) allowing the formation of conductive lines.[60] Recently,[61] self-aligned fully printed TFTs on PET foil with a minimal gate to source-drain overlap of 0.47 µm have been reported. In this case, self-alignment was obtained by wetting-based roll-off techniques of the droplets from previously patterned layers.

In summary, inkjet printing is a versatile, non-contact patterning technique with a resolution down to 20 µm. It is a fast technique often combined with other patterning strategies. Examples of combinations with mass-printing techniques have been given in the previous sections. Combination with high-resolution patterning strategies will be given in the following sections. Furthermore, digital mastering reduces processing costs and allows fast changes to the design.[10] Drawbacks of the technique are the necessary adjustment of the ink viscosity, concentration and solvent system to the nozzle (to prevent clogging) and the substrate material. Spreading of the ink and wanted or unwanted merging of dispensed droplets needs to be controlled. Further fine-tuning of solvent, concentration and viscosity is required to control the shape, thickness and morphology of the evaporated droplet.

## 2.3 High-Resolution Patterning

With conventional printing techniques, only a resolution of around 10 µm can be obtained, limiting the bandwidth to 10 kHz for printable semiconductors with a typical mobility of 0.01 $cm^2V^{-1}s^{-1}$.[62] Advanced and flexible electronic devices demand high-resolution patterning techniques.

When taking OTFTs as an example, high-resolution patterning would result in a larger bandwidth and higher switching speed while the geometric (parasitic) capacitance, the operation voltage and power consumption will be reduced. In addition, an improved on/off ratio at lower costs with a higher yield on smaller areas is possible.

In general, two types of high-resolution patterning techniques can be distinguished: top-down and bottom-up. In top-down, various lithography methods are miniaturized to pattern nano- to micronscale patterns. Photolithography and scanning beam (or maskless) lithography (e.g. electron beam and focused ion beam lithography) are the main patterning techniques in this area. The most known and widely spread patterning technique in semiconductor industry is optical lithography, which is therefore the only technique that will be covered in the following sections.

### 2.3.1 Photolithography

Photolithography (and its descendants) is the main patterning technique of the semiconductor industry. It proved to be far more capable of reducing the minimal feature dimensions to fulfill Moore's law than one could have imagined. In the 1960s through the mid-1980s, mercury lamps were utilized as light source, producing light across a broad spectrum with several strong peaks at 436 nm ("g-line"), 405 nm ("h-line") and 365 nm ("i-line"). Light filters allowed specific selection of the required spectral line to ideally match to the photoresist. The request of the semiconductor industry for denser and faster chips was met by the development of excimer laser lithography in 1982 by Kanti Jain[63, 64] at IBM, leading in the end to the steppers and scanners as primary patterning tools used in microelectronics production of today's world. Today, the world's leading provider of lithography systems for the semiconductor industry ASML, has started commercializing their pre-production, extreme ultraviolet lithography tool NXE:3100.[65] The tool is based on 13.5 nm wavelength

technology, patterning according to their roadmap at a resolution of 16 nm.[66]

In the following lines, the basic principle, developments and limitations of photolithography are described. Thereafter, the main challenges of transferring this technology and derivatives to flexible foil will be discussed.

In photolithography, patterns are made by exposure of a thin layer of a photosensitive lacquer (i.e. photoresist) on a substrate through a mask. The photomask is usually made of glass and a thin, light-blocking layer, typically made of chromium. Light exposure induces a chemical change of the light-sensitive material, changing its solubility in a developer solution. For positive tone resists the exposed, and for negative tone resists the unexposed regions are removed upon developing, resulting in a three-dimensional replica or inverted replica of the photomask on the substrate. The patterned photomask can be used in a subsequent process step as etch mask in order to define features on the wafer (Figure 2.8).

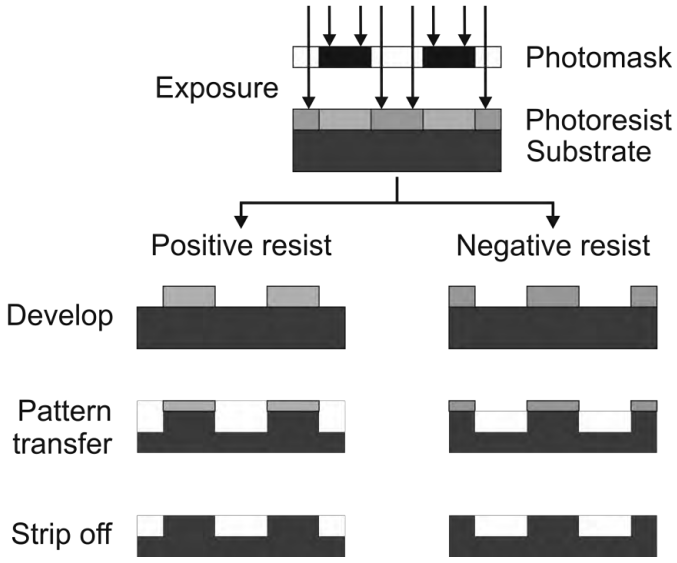


**Figure 2.8** Lithographic processes for positive and negative tone photoresists.

Photolithography has a couple of limitations. The minimal resolution *R* (i.e., critical dimension *CD*), given by the Rayleigh equation (equation 2.1), is

diffraction limited to the wavelength $\lambda_0$ in vacuum of the irradiating visible or UV light by the Rayleigh coefficient of resolution $\kappa_1$ and the refractive index $n$ of the incident medium, divided by the angular aperture $\theta$ of the lens system. The product $n \cdot \sin\theta$ is also known as the numerical aperture ($NA$) of the imaging system. The factor $\kappa_1$ is a process-dependent parameter that is determined by illumination conditions, mask technology, and photoresist capabilities with a lower limit of 0.25 for single-exposure optical lithography.[67]

$$R = \frac{\kappa_1 \lambda_0}{n \cdot \sin\theta} \tag{2.1}$$

The resolution limit of optical lithography has been continuously improved by reducing the exposure wavelength and increase of the numerical aperture. High-end optical lithographic patterning techniques such as deep- and extreme UV,[68] X-ray[69] and immersion lithography[67, 70] have pushed the resolution limit into the sub-micrometer and tens of nm regime on Si substrates.

On flexible substrates, photolithography is often used to pattern large micrometer features such as a gate or source-drain terminals,[71, 72] but also the semiconductor is regularly patterned by photolithography.[73] Flexible, all-polymer FETs have been fabricated by exposing a conducting polymer mixed with a photoinitiator through a photomask with deep UV radiation, rendering the exposed polymer non-conductive.[74]

### 2.3.2 Towards Alternative Methods for High-Resolution Patterning

Photolithographic processing requires many steps, is subtractive, and only suitable for patterning small areas.[75] The substrates and organic electronic materials are exposed to corrosive etchants, high-energy radiation, and relatively high temperatures during processing. The high investment and operation costs of photolithographic processing at the

resolution limit, are feasible as long as high yields and volumes are targeted. An economically more feasible route to high-resolution electronic devices is envisioned by one of the next-generation lithography techniques (e.g. nanoimprint lithography) on low-cost, polymeric foils. These alternative, high-resolution patterning techniques can be operated at lower costs to obtain the same or an improved resolution compared to the high-end photolithography systems. The integration in high-throughput patterning facilities such as a R2R line, would allow the fabrication of low-cost, large-area, flexible and lightweight devices. However, the transfer of processes from Si to polymeric foils is challenging and not straightforward.

Flexible electronic materials and interconnects offer thinner, lighter, highly compact end-products, and, often, a better performance.[76] Thin-film polymeric foils with a typical thickness of 25–200 μm are made of polyester (PE), polyimide (PI) or polycarbonate (PC).[77, 78] PE, and then mainly PET and PEN, are often used[79-81] and well-studied,[82, 83] showing a reasonable good mechanical stability and resistance to oxygen and water vapor penetration. Protection of the mainly organic materials of the electronic device from moisture and oxidation can be enhanced by barrier layers, additionally deposited on the foil. Barrier layers can also increase the chemical resistance of the polymers. The most stringent restriction to the patterning process and materials is the limited temperature window. The low glass transition temperature of the polymeric foils (e.g. ~70-85°C for PET[84]) requires alternative deposition techniques and newly engineered materials. As examples of recently developed, low-temperature materials, a high-*k* dielectric from titanium dioxide[85] and highly conductive self-sintering silver nanoparticles[58] have been reported. The second effect of temperature elevation on the polymeric substrates is a reduced dimensional stability due to a high coefficient of thermal expansion, even for biaxially oriented and thermally stabilized foils.[86] The dimensional stability and waviness of the foils can be improved by a bond-debond approach, temporarily laminating and flattening the foil to a carrier (e.g. Si or glass). These foil-on-carriers (FOCs) supply a stable platform for foil processing, but many new variables are introduced (e.g. bowing) and need

to be studied and tuned.[25, 86-90] Other bonding strategies developed are Electronics-on-Plastic by Laser Release (EPLaR) by Philips Research,[91] and Flexible Universal Plane for Display (FlexUPD) by ITRI.[92] In EPLaR, PI is coated on display glass as used in TFT-LCD processing plants. A regular TFT matrix is formed on top of it, whereafter the flexible display is released using a laser, allowing also reuse of the glass. In FlexUPD, PI is deposited on glass substrates with local debonding areas. A device (e.g. AMOLED) is patterned over the debonding area, allowing simple and quick cut-out of the patterned device with a slot die coater. The glass carrier cannot be reused however. For mass production, a prototype of an automated flexible-substrate debonding apparatus facilitated with a vacuum system has been reported by ITRI.

The limitations of conventional patterning resulted in the development of new or "alternative" nanopatterning strategies. Amongst these are soft lithography and nanoimprint lithography (hot embossing and UV NIL).

## 2.4 Soft Lithography

Soft lithography[93, 94] is a collective term for a set of techniques to pattern substrates from the micro- to nanoscale using an elastomeric stamp or mold,[93] typically made of PDMS. A variety of techniques has been developed and named after the utilization of the soft mold. In soft lithography, patterns are formed by printing inks, embossing microstructures, and replica molding by any of the following techniques:

- Microcontact printing (μCP)[95]
- Micromolding in capillaries (MIMIC)[96]
- Nanotransfer printing (nTP)[97-99]
- Replica molding (REM)[100]
- Microtransfer molding (μTM)[101]
- Solvent-assisted micromolding (SAMIM)[102]

Only the main soft-lithographic techniques (μCP, MIMIC, and nTP) utilized to pattern electronic devices on flexible foils will be further introduced and the obtained results discussed in the following sections. To complete the overview, the basic principles of the non-discussed soft lithographic patterning techniques REM, μTM and SAMIM are illustrated in Figure 2.9.

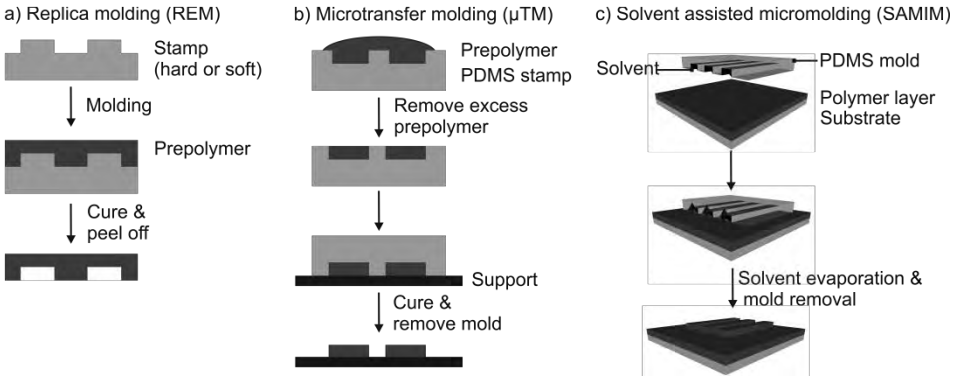


**Figure 2.9** Schematic illustration of the soft lithographic patterning techniques: a) replica molding, b) microtransfer molding, and c) solvent-assisted micromolding.

## 2.4.1 Microcontact Printing (μCP)

Microcontact printing (μCP) (Figure 2.10) is probably the best known soft-lithographic patterning technique. Invented by Whitesides et al. in the beginning of the 1990s,[103] this remarkably simple patterning technique is employed to form routinely self-assembled monolayers terminated with different chemical functionalities with (sub)micron lateral dimensions.[93] In short, a flexible, elastomeric stamp (typically made of PDMS) with patterned reliefs is inked by an alkanethiol solution. After drying, the stamp is pressed gently against a gold-coated substrate (or other thiol-compatible surface, e.g. silver or copper). Conformal contact between stamp and substrate ensures the transfer of the ink molecules to the substrate, forming rapidly a self-assembled monolayer (SAM) in the contact areas. In a subsequent step, the patterned SAM can be used as etch mask to transfer the pattern into the underlying gold, or a second SAM can be deposited by backfilling.

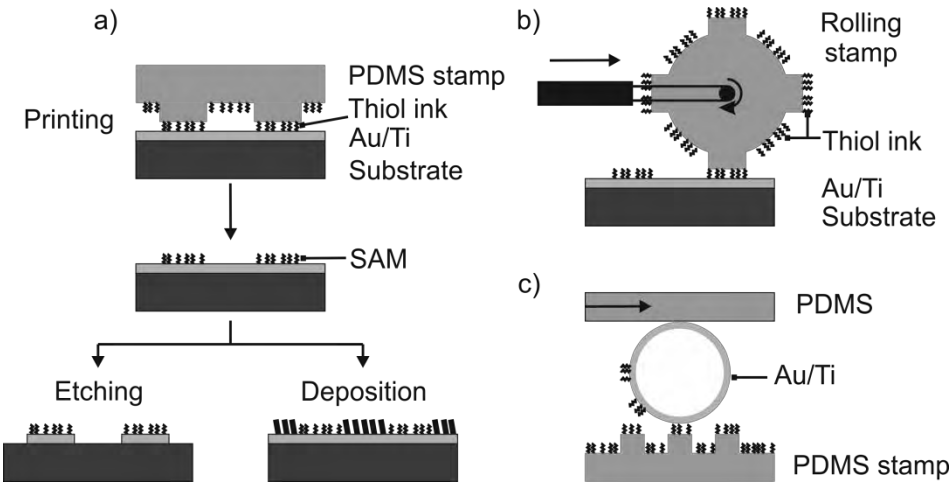


**Figure 2.10** Schematic illustration of various μCP processes, transferring an alkanethiol to a gold substrate by (a) single printing with a PDMS stamp, (b) continuous printing with a PDMS roller stamp, and (c) printing on a nonplanar surface. Images based on [93].

μCP is not restricted to the transfer of thiols to gold. Silanes, organic or inorganic species, biomolecules, and all sorts of materials can be transferred as inks.[104] As an example of alternative inks in the area of flexible electronics, the printing of Al-porphyrin SAMs on carboxylic groups formed on plastic foils (PET, PEN, PI) upon oxidation and on inert polymers (i.e. PE, polypropylene (PP) and poly(tetrafluoroethylene) (PTFE)) has been reported.[105] The patterned Al-porphyrin was used in a subsequent step to selectively deposit palladium-tin colloids, initiating Cu growth by electroless deposition (ELD). Also other SAMs have been printed on PET foil to induce Cu growth by ELD, resulting in Cu wires with a resolution of 0.45 to 10 μm.[106, 107] Microcontact printed SAMs can also be used to induce a wetting/dewetting contrast on a substrate for selective deposition of a sacrificial resist layer in a lift-off procedure to pattern metals.[108, 109] In a wetting-controlled, parallel, low-temperature process, although only demonstrated on Si wafer, μCP was used to pattern a "molecular template" on the substrate directing thin films by spincoating into the desired pattern to fabricate TFTs.[110] Contact printed, organic active matrix backplanes on 5 x 5-inch PET sheets,[111] with 10 μm wide and 20 μm-spaced source and

drain electrodes forming bottom-contact transistors, have been demonstrated as well (Figure 2.11).

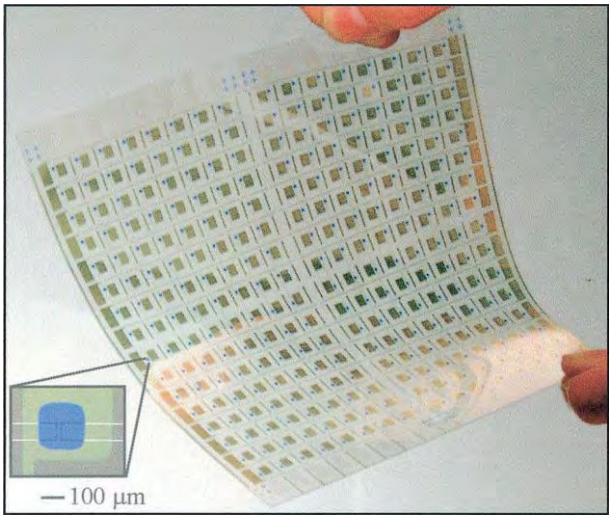


**Figure 2.11** Image of a completed plastic active matrix backplane circuit, patterned by µCP. The inset shows an optical microscopy image of a typical transistor [111]. Copyright © 2001 National Academy of Sciences, U.S.A.

## 2.4.2 Micromolding in Capillaries (MIMIC)

In micromolding in capillaries (MIMIC) (Figure 2.12), first reported by Whitesides et al. in 1995,[96] capillaries are formed by placing a soft elastomeric stamp, usually made of PDMS, with parallel protrusions on a smooth surface. The grooves form channels (capillaries), which are spontaneously filled with a solution as an effect of capillary pressure upon placement of a drop of the solution at the open end of the capillary. The filling speed is proportional to the cross-sectional dimensions of the channel and inversely proportional to the length of the channel containing the liquid and to the viscosity of the liquid.[112] After complete solvent evaporation or, in case of a low-viscosity polymer precursor after crosslinking, the stamp is removed leaving the patterns on the substrate.

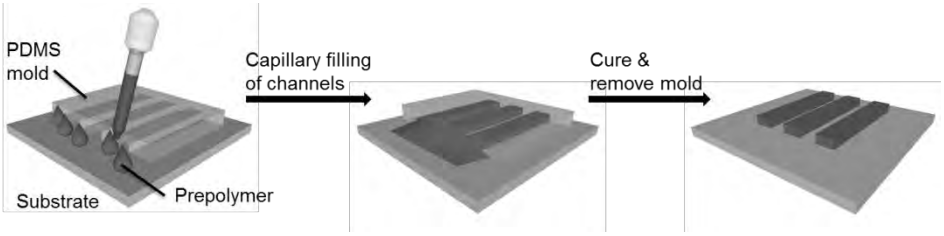


**Figure 2.12** Schematic illustration of micromolding in capillaries.

Upon gradual solvent evaporation in the channels, a meniscus is formed under the roof of the stamp channels by capillary forces. Depending on the solute concentration, two kinds of patterns can be obtained. In the high concentration regime, the solution reaches supersaturation when the channel is still filled with solution, resulting in deposition of solute on the entire bottom of the channel. In the dilute concentration regime, supersaturation is reached when most of the solvent is evaporated, and the volume of the residual solvent is not enough to completely fill the channel. In this case, the meniscus forms a U-[113] or W-shape[114] in the channel, dragging under capillary force the solute to the edges of the channel, where it accumulates and aggregates thereby forming defects in the stripes or creating split lines.[115] Specific polymers (e.g. polyaniline, polystyrene) can however, at slow solvent evaporation speed at room temperature, replicate the entire mold dimensions even from very low concentrated solutions of ~1%.[116] They need to undergo a transition to a dispersion in the channel from which polymer chains precipitate out as very small particles. The small particles aggregate upon attractive forces into nucleation sites. Particle influx from the larger reservoir at the channel entrance to the nucleation sites is generated to compensate for the loss of solvent upon evaporation. As an example, lines of polyaniline (emeraldine base) with a resolution between 350 nm and 50 µm were formed by MIMIC. After patterning, the emeraldine base was protonated with an acid to the electrically conductive emeraldine salt. With these polyaniline lines, all-plastic field-effect transistors (FETs) have been fabricated on PE substrates.[116] Due to the mechanical instability of the soft polymeric stamp, the dimensions of the channels in MIMIC are typically limited to about a few hundred nanometers.[117] A similar process of patterning a

precursor material with MIMIC on a flexible substrate, and transition into a conductive material after stamp removal, has been reported for graphene oxide.[118] With a hard PDMS stamp, centimeter-long and large-area 10 μm wide, ultrathin (1-3 nm) microwires of reduced graphene oxide flakes (500 nm to 1.5 μm) have been patterned by MIMIC of graphene oxide in aqueous solution on 3-aminopropyltriethoxysilane (APTES)-treated substrates ($SiO_2$ wafer, quartz, and PET), followed by a chemical reduction with hydrazine vapor. With the resulting microwires, front-gate FETs have been fabricated that have been used for sensing applications. Also free-standing films or polymer networks with a resolution of 1 μm can be created by simply dissolving (e.g. dissolving a $SiO_2$ sacrificial layer with HF), melting or vaporizing the solid support after MIMIC.[96]

### 2.4.3 Micro and Nanotransfer Printing (μTP and nTP)

In transfer printing[97-99] (Figure 2.13a), a functional layer is picked up by a rigid or elastomeric mold from one substrate and transferred as continuous[119] or patterned film[120, 121] to a second substrate. The substrate's adhesion energy needs to be carefully selected, allowing pick-up of material from the first substrate by the mold and deposition onto the second. The adhesion energies can also be adjusted by chemical functionalization. Depending on the patterning scale, the technique is referred to as micro- or nanotransfer printing (μTP[122] or nTP). The feature height of the stamp is in the range of 0.2–10 μm, and the width is between 0.05 and 100 μm.[97]

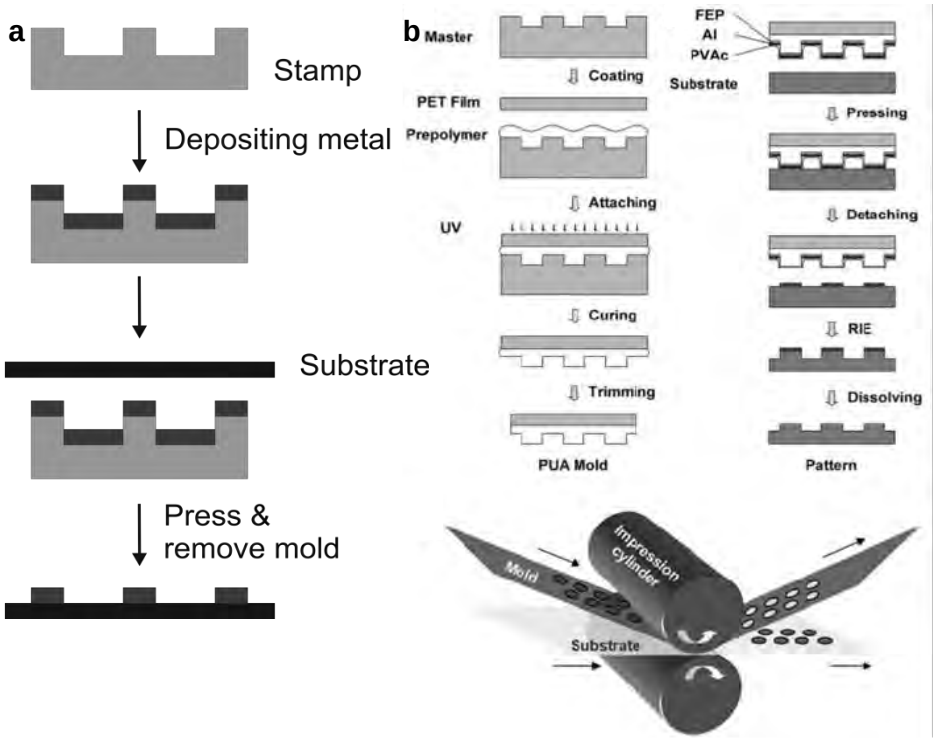


**Figure 2.13** Schematic illustration of (a) micro- and nanotransfer printing and (b) the fabrication and utilization of a rigiflex mold [123]. Copyright © 2005 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

Molds made of UV-curable poly(urethane acrylate) (PUA), so-called rigiflex[124, 125] molds (Figure 2.13b), were rigid enough for sub-100 nm patterning[126] and yet flexible enough for large-area application in R2R processing. Small molecule and polymer semiconductors for device applications are typically patterned by transfer printing. They are sensitive to oxidation in air and/or show a performance dependence on the polymer microstructure, substrate roughness, film deposition conditions, and solvent exposure.[121] The advantage of transfer printing in this case is the absence of process steps that partially can degrade the organic semiconductor or polymer, such as photoirradiation or exposure to incompatible chemicals (e.g. etch solutions), or solvents. Hines et al.[78, 127, 128] added the basic concept of NIL[129, 130] to nTP, patterning all components (metal, dielectric and semiconductor) of a TFT on plastic substrates (latex, nitrile, polyvinyl chloride (PVC), PET and poly(methylmethacrylate)

(PMMA)). Organic materials allowing processing near or above their glass transition temperature, were successfully transferred by proper adjustment of the heat and pressure during the thermal NIL process. Bottom-contact, bottom-gate TFTs with a PMMA dielectric layer, Au source-drain and gate electrodes and three semiconductor films from different classes (pentacene (small-molecule), P3HT (polymer), and carbon nanotubes (CNT) (macromolecule)) have been patterned on PET foil. John Rogers and coworkers continuously extend the patterning capabilities of nTP. They have reported on patterning of new materials (large-area flexible 3D optical negative index metamaterials[131]), and on transferring fully formed MOSFETs with thermally grown gate oxides and constructing integrated circuits to basically any substrate.[132]

The strong point of soft lithography is also the technique's weakness. The elastomeric character of PDMS results in stamp deformation upon contacting and during stamp removal. At high aspect ratios, defined as the height divided by the width of the features, buckling or pattern collapse of the elastomeric features can occur owing to gravity, adhesion and capillary forces,[133] generating defects in the pattern to be formed. Low aspect ratios result in sagging as a result of the compressive forces typical of printing and the adhesion between the stamp and the substrate.[93] An aspect ratio between 0.2 and 2 of the relief structures on PDMS surfaces is required to obtain defect-free stamps.[134] Other technical issues for the application of PDMS are the swelling when in contact with nonpolar solvents and the shrinking of about 1% upon curing.[135] An accurate registration for patterning multilayers is also more difficult with a flexible stamp than with a rigid stamp. Next to the general challenges of soft lithography, each technique has its own specific limitations. A drawback in μCP is for example diffusion of the SAM-forming molecules to areas not contacted by the PDMS stamp, broadening the feature itself and blurring the feature edge. With MIMIC, it is difficult to replicate the entire channel in case of a high aspect ratio. Line splitting can occur, breaking up the film in wide channels to result in splitted patterns and a non-flat feature profile. Line splitting can also be willingly used to fabricate thin lines at the channel

sidewalls, but control over the morphology is limited and avoiding line ruptures is a challenge. Furthermore, only low-viscosity inks in structures exhibiting a capillary force can be patterned. Arrays of individual dots for example, do not offer an open side for liquid influx. Nanotransfer printing allows selective transfer of materials to a wide range of substrates, making it a very broadly applicable patterning strategy, especially in combination with rigiflex molds. However, this printing technique requires precise adjustment of the intrinsic surface energies or adjustment by chemical modification or topography, to direct the transfer from the mold to the first or subsequent substrates.

## 2.5 Nanoimprint Lithography

In thermal nanoimprint lithography (NIL) (Figure 2.14a),[136, 137] a technique developed by Chou et al.,[129, 130] a rigid mold, typically made of Si, is pressed for a predefined time into an amorphous polymeric resist at a temperature typically 50-70°C[136] above the glass transition temperature ($T_G$). The resist suddenly turns low-viscous above $T_G$, by altering the mechanical and thermodynamic properties of the polymer.[138] The mold protrusions are thereby filled with resist by squeeze flow (pressure is the driving force to displace the viscous resist) and capillary forces (surface energy controls the wetting and spreading of the viscous resist) until it conforms to the surface relief of the mold.[136] Typically, a highly fluorinated SAM (e.g. *1H,1H,2H,2H*-perfluorodecyltrichloro-silane)[139] is applied as an anti-sticking layer to facilitate easy demolding and complete transfer of resist. Intrinsically, low-energy molds with high mechanical strength have also been reported, for example made of Teflon AF 2400 ($T_G$= 240°C).[140] Demolding occurs after reducing the temperature below $T_G$ and release of pressure. A thin residual layer remains on the imprinted substrate, which is removed by anisotropic reactive ion etching (RIE). The opened windows in the resist layer can be used to etch uncovered parts of an underlying layer (e.g. metal) in a direct etch process. Material (e.g. metal) can also be deposited after residual layer removal, followed by a lift-off step dissolving

the resist and the material deposited on top of it. With direct etching, an inverted pattern and with lift-off, a replica of the original mold pattern is obtained. Control over pattern replication and residual layer thickness has been improved by the development of UV-based nanoimprint lithography (UV NIL) in 1996,[141] and the further development into step-and-flash lithography (SFIL) by Wilson et al.,[142] crosslinking a low-viscosity resist by UV irradiation through a fused silica mold (Figure 2.14b). UV NIL allows room temperature imprinting at low pressure with good control over the residual layer thickness, making it (also) an ideal tool for patterning on foil.

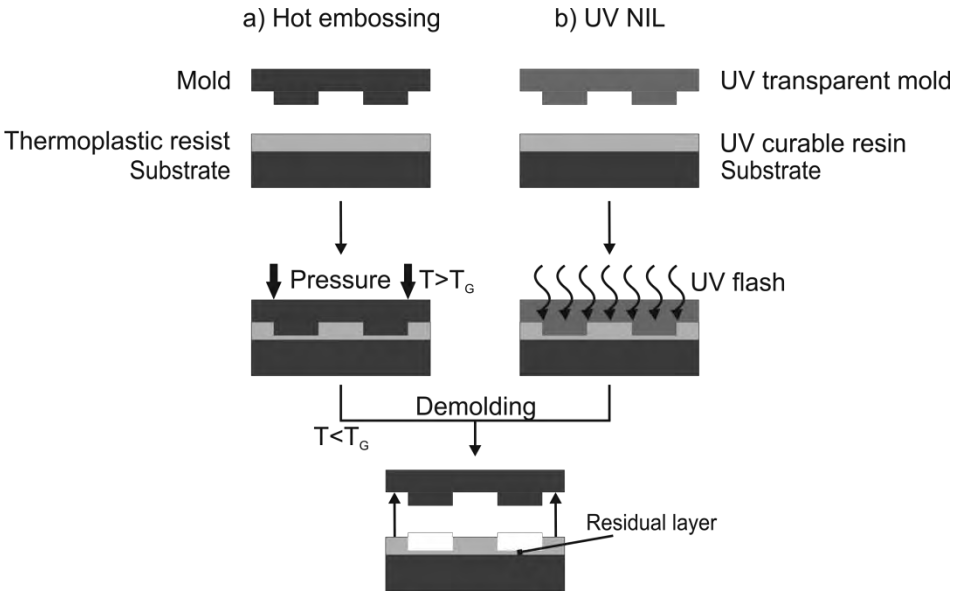


**Figure 2.14** Schematic illustration of nanoimprint lithography (NIL) of (a) a thermoplastic resist by hot embossing and (b) a UV curable resin by UV NIL.

NIL has been pointed out as one of the ten next-generation lithography techniques addressing the need for low-cost, high-resolution and high-throughput manufacturing of high-density integrated circuits and optics. In addition to the fabrication of rigid microchips, NIL can also be used as structuring technique in the fabrication of flexible electronic devices. For example, flexible OTFTs with source-drain contacts defined by thermal NIL[143] have been reported. Over the past 16 years, a variety of NIL processes has been developed, concerning different types of substrates,

resist materials and molding processes. Semi-continuous and continuous imprinting techniques, such as step-and-repeat imprint lithography (step-and-stamp IL[144, 145] for thermal resists, step-and-flash IL[142] for UV resists) and R2R NIL[146] have been invented for an increased throughput. Nonflat surfaces can be patterned with rigiflex molds[125] and reverse NIL (rNIL).[147, 148] Small and large features can be patterned by hybrid solutions combining NIL and conventional photolithography (combined nanoimprint- and photolithography; CNP).[149]

Complex electronic devices demand a good registration and overlay control in the patterning process. In OTFTs for example, the overlay of the source-drain and gate layers is important in order to reduce parasitic effects. Optimal alignment and therefore minimal gate overlap can, especially for R2R processes, only be obtained with a self-aligning patterning strategy. The critical overlay can thereby be obtained by "programming" one of the functional layers (e.g. gate) to define the next layer, or a multilevel etch mask defining all following layers can be fabricated on the substrate. In self-aligned imprint lithography (SAIL),[145-152] the entire material stack is deposited on the flexible foil whereafter a single, three-dimensional imprint is made defining all layers of the electronic device. The individual layers and structures of the device are patterned by smartly switching etch processes, opening one layer after the other using the just opened layer as etch mask and the next layer as etch stop. As an example, individual and arrays of bottom-gate transistors with amorphous silicon and transition metal oxides as active layer have been made on a web of 50 µm thick PI.[150, 153] A UV-curable resist is thereby patterned with a PDMS mold wrapped around a drum replicated from a patterned Si master. Fabricating a PDMS mold from a Si master mold allows numerous replications of the expensive master, without affecting its properties. The fabrication of a multilevel imprint mold in a two-step photolithographic and RIE process for top-gate a-Si TFTs has been reported and demonstrated on Si substrates.[154] Stadlober et al.[62] introduced a self-aligning technique that utilizes a thermal or UV NIL-patterned Al gate as photolithographic mask in a backside exposure step to define the positions of the source and drain in a

photoresist. Following shadow evaporation of the source-drain metal, the photoresist remaining exactly above the gate is removed by lift-off. A minimal overlap of 25-30 nm has been obtained.

For high-throughput, large-area fabrication of flexible electronics, both sheet-to-sheet (S2S) and R2R NIL (e.g., Roller NIL[155]) configurations seem suitable. An extensive review of continuous roller micro- and nano-patterning has been very recently reported by Dumond,[156] giving a good overview of this large-area imprint strategy. Therefore, only a brief summary will be given here. Two types of continuous imprinting exist, distinguished by the type of roller mold. Most often, the roller mold is patterned (Figure 2.15a). This can be done either directly,[157] or by patterning a flexible sheet mold[158-160] or shim and wrapping, or respectively mounting to a blank roller.[29, 161-163] Also, patterned molds spanning several rolls have been fabricated, so-called belt molds.[146] Alternatively, the roller mold can be used to apply pressure to a flat (Figure 2.15b) mold.[155] The latter suffers from similar scaling limitations as batch mode imprinting, in that the mold still has to be scaled to the full size of the substrate.[156] Furthermore, a classification in thermal[164] and UV-roller NIL (Figure 2.15c)[159, 160, 162] can be made like in batch patterning.

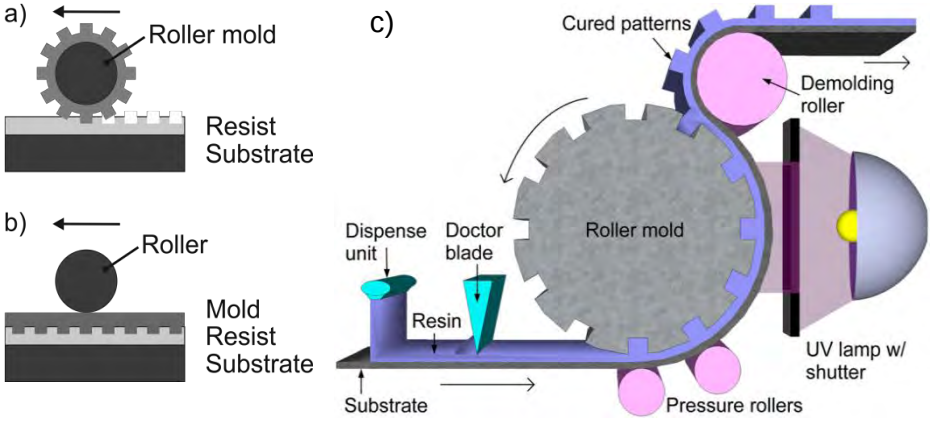


**Figure 2.15** Schematic illustrations of various types of roller NIL, with (a) a patterned roller mold and (b) a flat mold pressed by a non-patterned roller. Based on [155]. (c) Example of a typical UV roller NIL setup. Reprinted with permission from [156], Copyright © 2012, American Vacuum Society.

Since the first introduction of sub-micron and nanoscale thermal roller NIL in 1998[155] and UV roller NIL in 2006,[151, 165] the community improved the field immensely. Nowadays, seamless roller molds[157] can be fabricated and web tension control systems adjust the influences of temperature, vibration and thermal expansion. Furthermore, resist formulations (especially for UV roller NIL[146]), deposition systems and substrate coatings have been designed or optimized for uniform deposition and spreading, resulting in thin and reproducible layer thicknesses. With a cylindrical mold, pressure is only applied at the contact line between roller and substrate, allowing a considerable decrease of applied pressure and reduced gas entrapment. The distortion span in the resist layer, caused by local defects (e.g. dust) and surface contours or topography, is also reduced by the small contact line width between roller and substrate. Furthermore, the diameter of the cylinder with respect to the feature dimensions should be sufficiently large, in order to prevent damage by demolding to the just imprinted patterns.[166] A typical overlay resolution for a recently built R2R manufacturing line is around 5 µm.[167] With thermal roller NIL, mainly (nano-)gratings[29, 155, 164, 167] have been patterned. UV roller NIL has been applied in applications such as gratings,[146, 164] micro-lenses,[159, 160, 165] 3D-microstructures with undercuts,[166] anti-reflective coatings,[158] and flexible electronics.[150, 151]

A new member of the imprint lithography family is Substrate Conformal Imprint Lithography (SCIL).[168] It was designed to bridge the gap between UV NIL with rigid molds for best resolution and soft molds for large-area patterning.[169] As a mold, a patterned high-modulus PDMS layer is bonded to a thin glass carrier of up to 6 inch covered with a low-modulus PDMS layer. The PDMS mold is replicated from a Si master mold, allowing numerous replications without affecting the original. The 200 µm thick glass carrier provides in-plane rigidity avoiding lateral mold deformation as well as sufficient out-of-plane flexibility. Sequential imprint pressure is applied by evacuating a grooved vacuum plate attached to the mold sheet, allowing entrapped air to escape. Capillary forces pull down the mold achieving contact and induce resist filling into the PDMS features.

Demolding of the mold occurs in a wave motion ("peel-off fashion") as well. UV- and sol-gel-based resists have been utilized for the fabrication of 2D and 3D photonic crystals[168-170] and lines with a minimal resolution of 135 nm.[171] Charged particle nanopatterning of 2D and 3D masters allowed the fabrication of SCIL molds and pattern transfer into sol-gel resist with a minimal resolution of 20 nm.[172] The throughput of sol-gel imprinting is strongly limited by the diffusion speed and uptake of the solvent by the PDMS mold. The small layer thickness of the sol-gel (~100 nm) in comparison to the PDMS mold (~0.5 mm) is reported to not saturate or swell the PDMS mold, and to diffuse out of the PDMS upon mold release. SCIL is a low-cost, high-resolution patterning technique with potential for large-area fabrication of electronic devices. Its defect-tolerant, room temperature and low-pressure process makes it an interesting patterning technique for flexible substrates. However, no studies have been reported in this direction to date.

## 2.6 Concluding Remarks

Large-area, high-throughput patterning of flexible electronic devices has gone through a rapid development in the past decades. With the promise of low-cost, light-weight, thin and bendable devices, commercial mass-printing techniques have been further developed and adjusted to meet the process restrictions given by the polymeric foil substrates. The mechanically instable and wavy foils limit most strictly the temperature budget of the process to below 150°C, due to generally low glass transition temperatures of low-cost foils. The use of other polymeric foils, such as PI in EPLaR[91] and FlexUPD,[92] allows higher processing temperatures. A reduced temperature window also puts pressure on well-established materials and fabrication processes in semiconductor industry. Low-temperature, or even better room-temperature, processes need to be engineered to deposit dielectrics with a high dielectric constant and to pattern and anneal metals or metal precursors. Thermal expansion mismatches between the polymeric foils and patterning molds or masters

need to be compensated for high-resolution and precisely registered printing. The polymeric nature of the foils makes them also sensitive to chemicals and aging or yellowing induced by (high-energy) irradiation. Organic compounds of the electronic device need to be protected from influences of humidity and oxygen by specially designed coatings or barrier layers. The limited resolution and quality of the mass printing techniques has led to the request for new, high-throughput R2R lines integrating more recently developed, alternative and high-resolution patterning soft and imprint lithography techniques. Especially for these high-resolution patterning strategies, the dimensional instability, deformations and variations in thickness of the foils contribute to the given challenges of developing large-area, flexible electronics patterned by a R2R strategy. Other than in batch mode, accurate registration and therefore alignment of a multilayer device is not possible or economically feasible to date. Self-aligning device architectures and processes need to be developed and integrated in R2R lines, while keeping the perspective of low-cost and high-throughput processing.

The mass printing techniques flexography, gravure, offset and screen printing, reviewed in the beginning of this chapter, have a long history in printing on paper and textiles, to which printing on polymeric foils can be added now. Each technique has its individual benefits and drawbacks, and therefore specified applications. Common benefits are the widespread and well understood processing steps and conditions required for large volumes to be printed, up to 2 $km^2/h$ for offset printing. A general and important drawback of these techniques, in particular for fast operating electronic devices meeting Moore's law, is the low resolution, typically down to 20 µm. Inkjet printing is a simple process and is easily combined with mass printing and high-resolution patterning strategies. It is a low-cost, non-contact, low-impact patterning technique benefiting from the flexibility of digital mastering. Digital printing is more customizable, produces less waste and reduces fabrication costs. Costs for the fabrication of a printing master range from relatively low-cost in screen printing to medium cost for rotary screen printing and flexographic printing to very

high costs for gravure printing. The resolution of inkjet printing is limited to approx. 20 μm. Ink parameters need to be carefully set to meet the required viscosity, spreading, merging and drying behavior for each type of substrate. The main yield-limiting factor in inkjet printing is nozzle clogging.

Photolithography is probably the most established patterning technique with an extreme resolution bandwidth. However, the high initial and processing costs combined with a relatively low throughput and patterning area make it less attractive for low-cost fabrication of large-area and flexible devices. Furthermore, substrates and organic materials are exposed to corrosive etchants, high-energy radiation, and high temperatures during processing.

The alternative, high-resolution patterning techniques developed in recent years with the aim to deal with the resolution limitations, exceeding costs and small patternable area of photolithography have been reviewed in the last part of this chapter. The family of soft-lithographic techniques allows large-scale, high-resolution patterning of thin and uniform layers on foil. However, no flexible electronic device singularly patterned by one of these techniques has been demonstrated. The low-cost, easily formable, and material-transferring mold material PDMS is mechanically instable under higher pressure and at high aspect ratios: features in PDMS tend to buckle, collapse or sag. Furthermore, PDMS swells in non-polar solvents and shrinks upon curing. μCP is mainly used to print a mask of a patterned SAM onto the substrate, leading in several subsequent steps to selective metal growth. The dimensions of regular microcontact printed features tend to increase and show blurred feature edges due to ink diffusion over the surface. With MIMIC, thin layers can be reproducibly replicated from low-viscous inks experiencing a sufficient capillary force upon channel filling. Channels with a high aspect ratio are usually not completely filled, leading to a concentration-dependent drying profile of the patterned line and/or line splitting and film break-up. nTP requires careful adjustment of surface energies, allowing pick-up of a prefabricated feature by PDMS from one

substrate and transfer to another substrate. In this way, the target substrate is not degraded by irradiation or exposure to incompatible chemicals due to fabrication and patterning on the first substrate. Even complete MOSFETs have been recently transferred to flexible and temperature sensitive foil.[132]

Nanoimprint lithography has been indicated on the ITRS roadmap as one of the ten next-generation lithography techniques addressing the need for low-cost, high-resolution and high-throughput manufacturing of high-density integrated circuits and optics. Numerous reports have shown the applicability of NIL to pattern at least part of an electronic device on rigid, flexible and non-flat surfaces. However, the dimensional bandwidth of simultaneously patternable features in NIL is not as wide as in photolithography. Resist flow is limited, and replication of high-aspect ratio features with the risk for air entrapment is difficult and slow. An additional risk in R2R imprinting of high-aspect ratio features, is the rupture or damage of the imprinted features by the peeling mode of demolding. Thermal NIL is less suited for high throughput processing than UV NIL due to thermal cycling and the risk of thermal expansion mismatches of substrate and mold. Removal of the residual layer, which is typical for NIL, is non-trivial, and should be circumvented by residual layer-free imprinting or used as integral part of the patterned device if possible. The development of R2R imprint with patterned or belt molds has raised the throughput immensely, and the first successful flexible electronic devices have been demonstrated. Key challenge in R2R NIL is the low-cost fabrication of seamless cylindrical molds of a sufficiently large diameter. Web tension and cleaning, continuous ink deposition and layer registration are other challenges in R2R processing. Minimal overlay and good layer registration are evident for fast switching and well performing electronic devices showing low parasitic effects, but they are difficult to control on the mechanically instable and wavy foils. Only self-aligned imprint lithography strategies can be a cost-effective solution for large-area patterning of multilayer devices. The new technology SCIL bridges not only the high

resolution obtained with hard molds and large-area processing obtained with soft molds, but it bridges also the batch mode of regular NIL strategies and the continuous mode of R2R. Its defect-tolerant, room-temperature and low-pressure process makes it an interesting patterning technique for flexible substrates. However, resist compositions have to be engineered for optimal and fast filling and replication behavior. Sol-gel systems seem not to meet the request for high-throughput patterning, due to the slow, solvent-diffusion dependent patterning.

The steadily increasing number of reports and applications in the area of high-resolution printing on low-cost flexible foils reflect the increasing interest of the community to fulfill the promise of low-cost, high-volume, high-throughput production in R2R processing lines. Promising electronic devices such as OLED-based displays, RFID tags, and OSCs are to be light-weight, thin and flexible, inexpensive and disposable. While microlenses and similar simple structures can be reproducibly fabricated today, more complicated, multilayered electronic devices are still a challenge. For every device architecture, a combination of the available deposition, printing and patterning techniques will need to be chosen to provide the most efficient process regarding throughput and costs. For example, high-resolution features will need to be patterned by NIL, but larger contacts can be easily printed by one of the more classical techniques. A universal patterning strategy for all applications seems unlikely. The resolution, processing temperature and throughput are the main limitations in the process. Dramatically coinciding with the resolution of multilayered devices is the overlay accuracy, a challenge probably only to be solved in a self-aligned assembly mechanism. From a materials perspective, cheaper but higher performing low-temperature processable (organic) materials will need to be engineered to meet the restrictions given by the patterning process and thermally sensitive foil.

## 2.7 References


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**Chapter 3**

# Double-Layer Imprint Lithography on Wafers and Foils from the Submicrometer to the Millimeter Scale

*In this chapter, a thermal imprint technique, double-layer nanoimprint lithography (dlNIL), is introduced, allowing complete filling of features in the dimensional range of submicrometer to millimeter. The imprinting and filling quality of dlNIL was studied on Si substrates as a model system and compared to results obtained with regular NIL (NIL) and reverse NIL (rNIL). Wavy foils were imprinted with NIL, rNIL and dlNIL and the patterning results compared and discussed. With dlNIL, a new application possibility was introduced in which two different resists having, for example, a different etch resistance to a certain plasma were combined within one imprint step. dlNIL allows extension to many resist combinations for tailored nanostructure fabrication.*

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## 3.1 Introduction

The fabrication of micro- to nanoscale structures of a wide variety of rigid and flexible materials is of large interest for the semiconductor industry and for nanoscience in general. Nanoimprint lithography (NIL),[1,2] first discovered by Chou et al.[3,4] is seen as one of the next generation lithography techniques addressing the need for low-cost, high-resolution and high throughput manufacturing of high-density integrated circuits and optics. In addition to the fabrication of rigid microchips, NIL can also be used as structuring technique in the fabrication of flexible electronic devices and it is suitable for large-area production in both sheet-to-sheet and roll-to-roll (e.g., Roller NIL[5]) configurations. The enhanced functionality (bendable, rollable) combined with the low-weight and possible transparency of flexible devices enables high-level integration into products and systems such as mobile phones, E-readers and thin-film transistor (TFT) displays. However, surface flatness and the dimensional stability of the flexible substrates need to be controlled to obtain good registration accuracy for multilayer devices, such as thin-film transistors.

A lot of NIL processes have been developed over the past 15 years, concerning different types of substrates, resist materials and molding processes. Continuous imprinting techniques, such as step-and-repeat imprint lithography (step-and-stamp IL[6,7] for thermal resists, step-and-flash IL[8,9] for UV resists) and roll-to-roll NIL[10] have been invented for an increased throughput. Nonflat surfaces can be patterned with rigiflex molds[11] or reverse NIL (rNIL).[12,13] Small and large features can be patterned by hybrid solutions combining NIL and conventional photolithography (combined nanoimprint- and photolithography; CNP).[14]

In imprint lithography, mold filling and polymer release are important factors to successful thermal embossing. Numerous studies have been carried out by a broad range of researchers,[15-22] discovering a strong dependence of polymer squeeze and shear flow as function of the cavity geometry, polymer film thickness and viscoelastic properties from the 10-

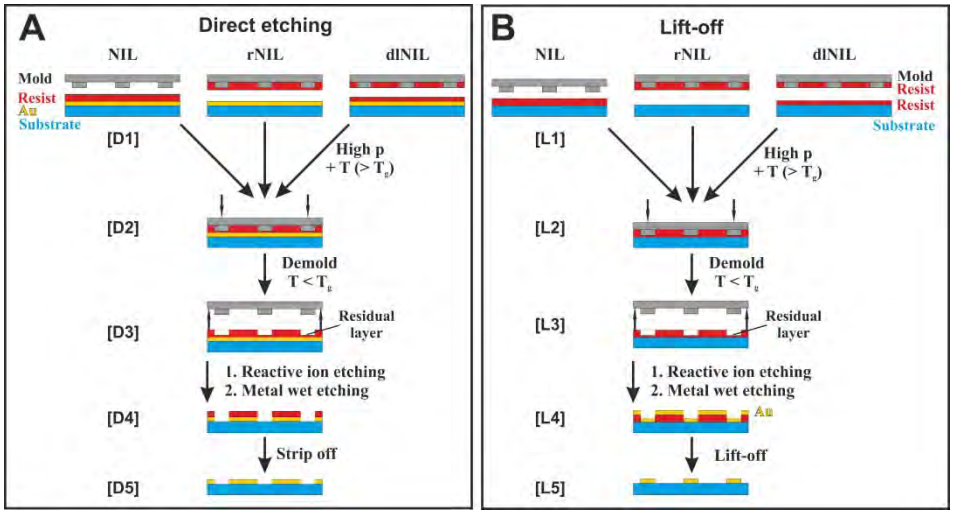
nm to the 1-mm scale. Depending on the architecture of the desired structure (aspect ratio, duty cycle) inhomogeneous single peak or dual peak deformation of the polymer occurs. Small cavities fill first, unless the local cavity width is less than the film thickness. In that case constrained single peak flow occurs.[23] The technique of rNIL was developed to overcome filling issues in large features, experienced with regular NIL. In rNIL, the resist is applied to the mold rather than the substrate. The resist fills the protrusions of the mold during deposition (e.g., spincoating) and is transferred to the substrate during imprinting. Arbitrarily sized features can be imprinted without filling issues. Simultaneous filling of small and large features over a wide dimensional range has not been reported for rNIL.

In this chapter, the resist filling behavior and simultaneous pattern transfer of features over a wide dimensional range, from the submicrometer to the mm regime, on rigid and flexible substrates such as commercially available thin plastic foils, are studied. Double layer NIL (dlNIL), a technique based on polymer bonding lithography developed by Borzenko et al.,[24] is used to combine homogeneous and heterogeneous resist layers applied to both the mold and the substrate. The mold filling quality and pattern transfer results on Si wafers are compared to imprint results obtained with the existing thermal imprint techniques regular NIL and rNIL. Pattern transfer results obtained by imprinting on nonflat surfaces (foils glued to a carrier) with NIL, rNIL and dlNIL are also compared and discussed. An interesting new possibility of the dlNIL technique is given: a patterned two-layer resist on rigid and on nonflat surfaces using different resists as top and bottom layer, thereby smartly making use of different etch rates or surface energies of the two resists for example.

## 3.2 Results and Discussion

### 3.2.1 Design and Process Scheme

Scheme 3.1 shows the process flows of the imprint lithography techniques discussed here, NIL, rNIL and dlNIL, displayed both in a direct metal etch ([D1-D5]) and lift-off ([L1-L5]) fashion. Depending on the imprint technique, the thermoplastic resist is deposited by spincoating on the substrate (NIL), on the mold (rNIL), or on both the substrate and the mold (dlNIL).




**Scheme 3.1** Process flows of NIL, rNIL, and dlNIL leading to (A) direct etching of an underlying metal layer or (B) a metal pattern after evaporation and lift-off. [D1]/[L1]: Resist is deposited on the substrate (NIL), the template (rNIL), or on both (dlNIL). [D2]/[L2]: Under the influence of pressure and temperature the resist is imprinted, followed by a demolding step below $T_g$. [D3]/[L3]: The residual layer is removed by anisotropic RIE opening windows in the resist layer. The inverse patterns are obtained by [D4] wet etching and subsequent [D5] resist strip-off. Patterns are obtained by [L4] metal deposition and [L5] subsequent lift-off.

Si wafers and 125 µm thick poly(ethylene naphthalate) (PEN) foils reversibly glued to a carrier (foil-on-carrier; FOC) were used as substrates. Substrates used in the direct etch approach were covered with a thin metal layer before resist deposition.

An antisticking layer, typically 1H,1H,2H,2H-perfluorodecyltrichlorosilane (PFDTS) or octadecyltrichlorosilane (OTS) (see below) deposited on the mold, is required to guarantee complete transfer of the imprinted resist to the substrate during demolding. The mold contains line and square features in the dimensional range of 1.0 µm up to 1.4 mm with a depth of 200 nm. The mold is pressed for a time $t_{imp}$ into the resist at a temperature $T_{imp}$ well above the glass transition temperature ($T_g$) of the thermoplastic resist ([D2] and [L2]). MrI7020E was chosen as a dedicated imprint resist with a $T_g$ (60 °C) well below the $T_g$ of PEN (120 °C). Above $T_g$, the viscosity of the resist lowers allowing the mold protrusions to be filled. After cooling down below $T_g$ demolding can occur, separating the template from the resist ([D3] and [L3]). A thin residual layer remains on the imprinted substrate, which is removed by anisotropic reactive ion etching (RIE) using $O_2$ plasma opening windows in the resist layer. In the direct etching process (Scheme 3.1A), the uncovered metal layer (30 nm gold and 5 nm Ti adhesion layer) is removed by wet etching ([D4]) and the process is finished by stripping off the resist in $O_2$ plasma or an adequate solvent ([D5]). When following the lift-off route (Scheme 3.1B), metal is deposited after residual layer removal ([L4]). The lift-off process is finished by dissolving the resist, simultaneously removing all metal deposited on top of it ([L5]). With direct etching an inverted pattern and with lift-off a replica of the original mold pattern is obtained.

### 3.2.2 Regular NIL

Regular NIL was applied on a Si wafer using an OTS-coated mold and mrI7020E ($T_g$= 60 °C) as the resist, at a pressure of 40 bar for 300 s at 140 °C. Demolding occurred at 55 °C.

The optical microscopy images in Figure 3.1 show regular NIL-patterned resist on Si. Features of 200 µm square pads connected to 5 µm wide and spaced lines were well replicated, showing a reasonably homogeneous residual layer and filling deduced from the absence of color deviations. The narrow 1 µm-spaced 10 µm-wide lines (b) and the large 1.4 mm square pad

(c) are replicated, both showing inhomogeneous filling effects (color deviations) and a secondary structure on top of the resist. A SEM cross section image of the edge of a NIL patterned 200 µm wide pad is shown in Figure 3.1d.

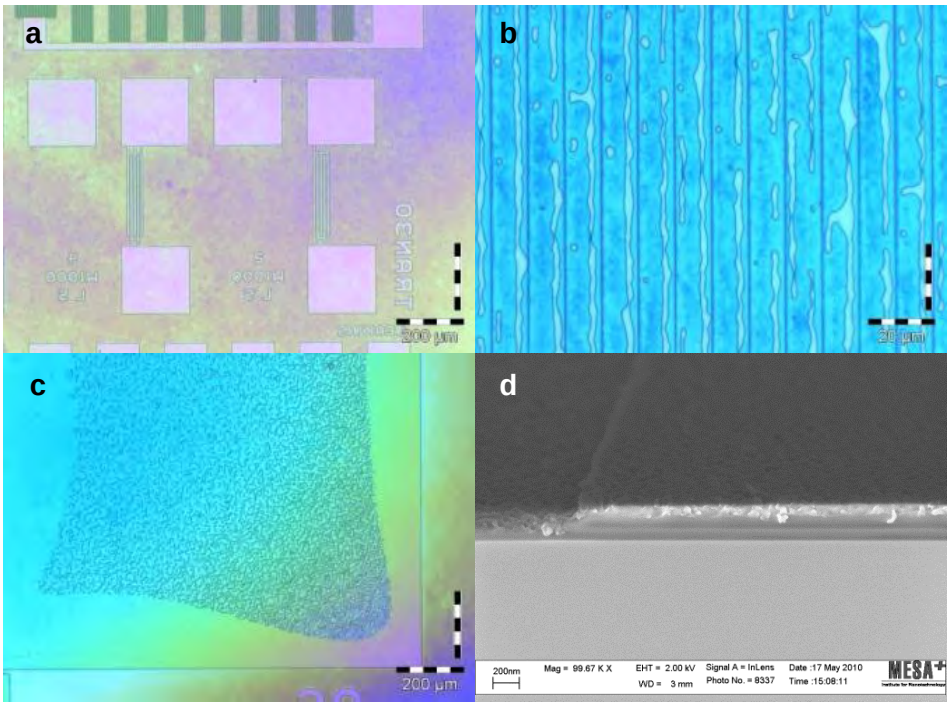



**Figure 3.1** (a-c) Optical microscopy and (d) SEM images of thermal NIL-patterned mrI7020E resist on Si with an OTS-coated template. (a) Interdigitated 5 µm spaced source-drain fingers connected to 200 µm contact pads. Dewetting patterns are visible on top of (b) the narrowest 1 µm spaced lines and (c) the largest 1.4 mm wide imprinted features. (d) SEM cross section image of the edge of a 200 µm wide feature patterned by NIL.

An improved filling might be obtained by raising the temperature and pressure even further, to improve the fluido-dynamic behavior of the high viscosity polymer. On the other hand, higher temperatures and pressures are undesirable characteristics in device fabrication, and alternative processes are more promising.[24]

The additional structures visible on the narrow spaced lines and on the large (>200 µm) features are attributed to the resist dewetting from the OTS antisticking layer of the mold (contact angle of 98.2 ± 0.3[25]) during

imprinting. Some structure resulting from this dewetting apparently remains on top of the imprinted features after demolding. Imprinting results obtained with a PFDTS antisticking layer, which has a lower surface energy (static water contact angle 109.6 ± 0.4[25]), showed a stronger dewetting effect. OTS and PFDTS showed both good antisticking layer properties, as all resist was in all experiments completely transferred to the substrate. No resist remained on the mold.

With regular NIL, (small) features in the dimensional range of 1 µm-~150 µm could be transferred with good reproducibility over the whole 4" Si wafer. Larger features (>200 µm) however, and unpatterned open areas were often incompletely filled as visualized by the color deviations in the optical microscope images in Figure 3.1.

### 3.2.3 Reverse NIL

In reverse NIL (rNIL),[12] the thermoplastic resist is spincoated on the template (Scheme 3.1). The advantage of this procedure is the direct filling of the cavities before imprinting, promising complete filling without suffering from a thinner resist layer in the center of large features. rNIL was applied on a Si wafer using an OTS-coated mold and mrI7020E as resist, under 40 bar pressure for 300 s at 140 °C. Demolding occurred at 55 °C.

Figure 3.2 shows optical microscopy images of rNIL-patterned resist on Si. Features of 200 µm up to 1.4 mm were entirely filled, not suffering from the incomplete filling observed during regular NIL. Also dewetting was no longer observed on the 1 µm-spaced, 10 µm-wide lines and on the largest 1.4 mm feature (Figure 3.2 b,c). Except for the largest features (Figure 3.2c), the residual layer thickness and imprint height appeared to be fairly homogeneous, as deduced from the absence of color deviations (Figure 3.2 a,b). A SEM cross section image of the edge of a rNIL patterned 200 µm wide pad is shown in Figure 3.2d.

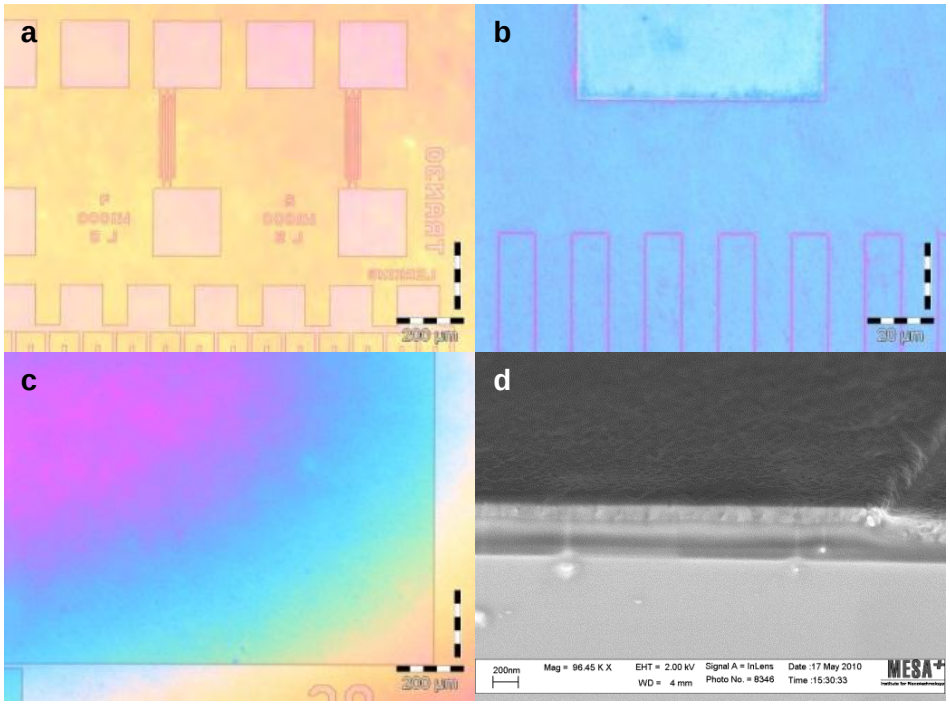



**Figure 3.2** (a-c) Optical microscopy and (d) SEM images of rNIL-patterned mrI7020E resist on Si with an OTS-coated template. All features over the entire 4 in. wafer were transferred and filled entirely. (a) Five-micrometer-wide interdigitated fingers connected to 200 µm contact pads. No dewetting patterns were observed in (b) the narrowest 1 µm spaced 10 µm wide lines and (c) the largest 1.4 mm features. (d) SEM cross section image of the edge of a 200 µm wide feature patterned by rNIL.

All features on the mold, from 1.0 µm to 1.4 mm, could be replicated with rNIL by use of an OTS antisticking layer, allowing completely and homogeneously filled mold protrusions. Initial imprints with PFDTS as antisticking layer, resulted only in partial transfer of small and large features with and without residual layer. An observed problem with rNIL is lack of resist transfer from not fully filled mold protrusions. If the resist does not contact the substrate during imprinting, it is not transferred and remains in the mold cavities.

### 3.2.4 Double-Layer NIL

In double layer NIL (dlNIL), a technique based on polymer bonding lithography,[24] a thin thermoplastic resist layer is spincoated on the substrate and on the mold. Above $T_g$ both resist layers merge. This constitutes a major advantage of dlNIL, as it allows the combination of two different resists (see below). With dlNIL, the resist present on the substrate flows into the not fully filled protrusions of the mold and combines with the resist spincoated on the mold. During demolding below $T_g$, the entire imprinted resist layer is transferred to the substrate, leaving no residues in the mold protrusions (Scheme 3.1).

For dlNIL, the resist was spin-coated on the substrate and on the OTS-coated mold, and was imprinted at 140 °C under 40 bar pressure for 300 s. Optical microscope and SEM images (Figure 3.3) show a range of features patterned by dlNIL on Si. For SEM imaging, 5 nm Au/Pd 80%/20% was deposited on top of the imprinted features. The 200 µm pads (a) and larger features of 1.4 mm (c) were entirely transferred, not suffering from opened windows in the middle of the features due to lack of filling during imprinting. Dewetting was no longer observed for the 1 µm-spaced lines (b) and the largest 1.4 mm features (c), similar to rNIL. Except for the largest feature (c), the residual layer thickness and imprint height appeared to be homogeneous. The SEM pictures (d-f) show the high quality of dlNIL-patterned interdigitated 5 µm-wide and spaced lines (d), a 1.4 µm-spaced line structure (e) and a SEM cross section image of the edge of a dlNIL patterned 200 µm wide pad (f).

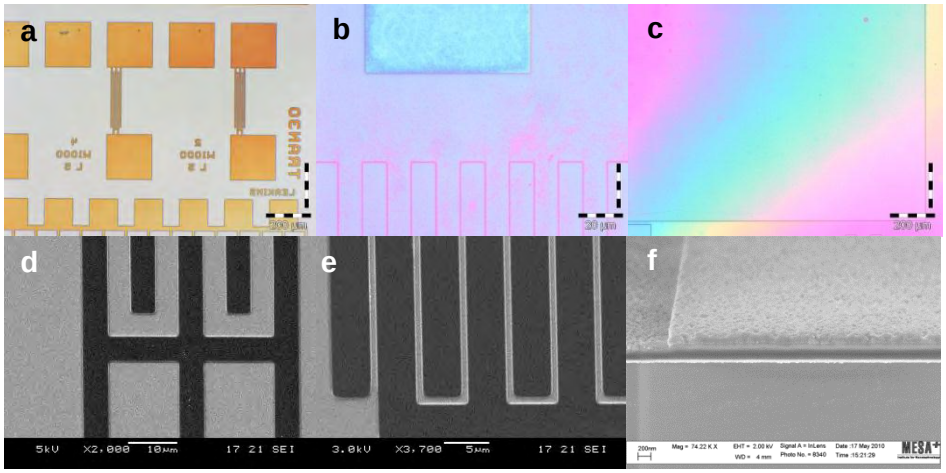



**Figure 3.3** (a-c) Optical microscopy and (d-f) SEM images of dlNIL-patterned thermoplastic resist on Si with an OTS-coated mold directly after imprinting. Resist mrI7000E in a 100 nm and a 200 nm layer thickness was applied on the mold, respectively the substrate. All features over the entire 4 in. wafer were transferred and filled completely without obvious dewetting patterns. (a, d) 5 µm-wide interdigitated fingers connected to (a) 200 µm contact pads. No dewetting patterns could be observed in (b) the narrowest 750 nm-spaced lines and (c) the largest 1.4 mm features. (e) SEM image of 1.4 µm spaced lines and (f) SEM cross section image of the edge of a 200 µm wide feature patterned by dlNIL on a gold coated Si substrate.

Figure 3.4 shows gold features visible on Si, made by dlNIL and subsequent wet etching and resist strip-off (Scheme 3.1A). The smallest patterned feature is a 4-point-probe architecture of a 1 µm-wide line connected to 125 µm-sized contact pads (a). Interdigitated lines of 5 µm width spaced by 2.5 µm in (b) and 4 µm wide lines spaced by 5 and 20 µm connected to 125 µm contact pads show the quality of dlNIL-patterned metal structures.

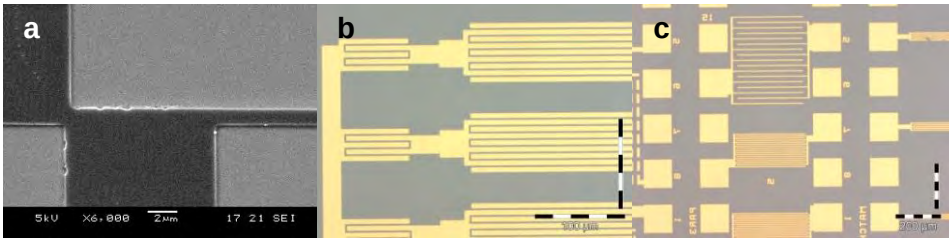



**Figure 3.4** dlNIL-patterned features with an OTS-coated mold on Si after residual layer removal with RIE, Au and Ti wet etching and resist strip-off. (a) SEM image of the smallest patterned line feature with a width of 1 µm. Optical microscopy images of (b) 5 µm wide interdigitated 2.5 µm spaced lines and (c) 4 µm wide, 5 and 20 µm spaced lines connected to 125 µm contact pads.

Thermal imprinting was not only performed on Si wafers, but also on 125 µm thick PEN foil reversibly glued to a carrier (foil-on-carrier, FOC). With NIL, rNIL and dlNIL these FOCs were patterned under the same conditions as their Si wafer counterparts using an OTS-coated Si mold at 140 °C under 40 bar pressure.

The flexibility and waviness of foils makes faithful pattern replication more difficult when compared to imprinting on Si substrates. With the FOC approach, the flexibility and waviness were drastically reduced to an overall waviness of 1.5 µm within the substrate. The difficulty lies in the inhomogeneous filling of resist in the hills and valleys of the foil, resulting in an inhomogeneous overall residual layer thickness. During RIE, the breakthrough of the residual layer occurs earlier on the hills (thinner residual layer) than in the valleys. Residual layer removal in the valleys therefore may occur concurrently with imprint pattern removal on the hills. The etching problem occurring for varying residual layer thicknesses is tackled by the combination of two different resists, as is discussed below.

Figure 3.5 shows optical microscopy images of resist patterned by NIL, rNIL and dlNIL on FOC. Cross sectional images by lamella cutting with focused ion beam (FIB) were unsuccessful due to the low $T_g$ (60 °C) of the imprint resist. The same sets of features are compared for all three techniques. Similar to the results obtained for patterning on Si with regular NIL, the larger (>150 µm) features could not be filled completely on FOC. Strong height differences in the resist layer thickness from the edge to the center of the feature are indicated by the color deviations in the optical microscopy images. Also here, this is attributed to two-peak filling behavior.

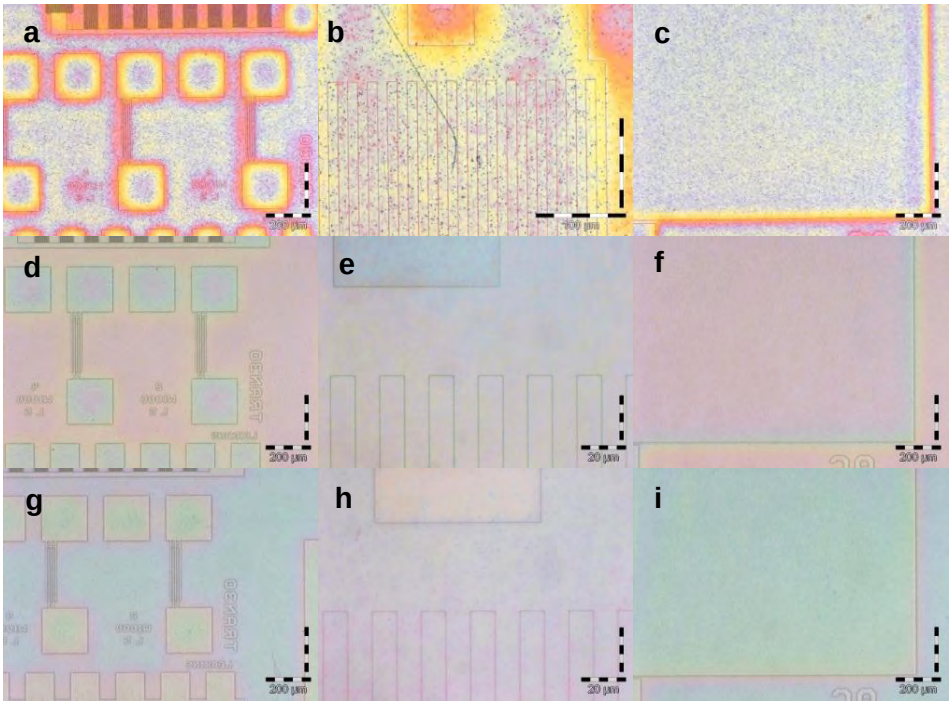
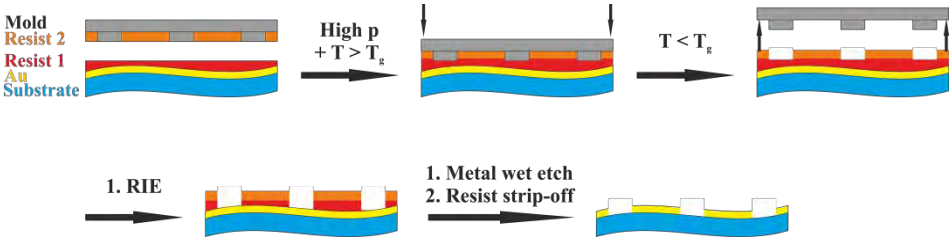



**Figure 3.5** Optical microscopy images of (a-c) NIL, (d-f) rNIL, and (g-i) dlNIL-patterned thermoplastic resist on FOC with an OTS-coated template. In (a, d, g) 5 µm-wide and spaced interdigitated fingers connected to 200 µm-wide contact pads, in (b, e, h) 1 µm-spaced lines and in (c, f, i) a part of the largest 1.4 mm wide feature are shown.

Imprinting with the rNIL and dlNIL techniques resulted in homogeneous resist and residual layer thicknesses and in pattern transfer of the entire imprinted range of 1.0 µm up to 1.4 mm features to the FOC with no major difference with respect to the filling quality. With NIL, inhomogeneous filling of the larger features, visible in the contact pads in Figure 3.5a, and the lowest patterning quality were observed.

With dlNIL it is not only possible to pattern with high quality over a large dimensional range features on Si and foil, but it also allows the combination of two resists with different properties. A potential application is shown in Scheme 3.2. A resist (resist 2), with for example a high oxygen plasma resistivity, is deposited on the mold, while a more oxygen sensitive resist (resist 1) is deposited on the substrate. Resist 1 fills the voids of not completely and homogenously with resist 2 filled protrusions on the mold.

Furthermore, the additional resist layer ensures a conformal contact between substrate and resist 2. An inhomogeneous resist layer thickness is often observed with wavy substrates (foil), as hills and valleys are differentially filled. The here shown, heterogeneous combination of two resists with dlNIL allows removal of the entire residual layer, benefitting from the higher etch resistivity of the top imprinted resist toward oxygen RIE, compensating the thinner residual layers on top of the hills of the wavy foil. Resist 2 can be etched, for example with fluorine-based plasma, until it breaks through to resist 1, after which $O_2$ RIE is used to etch resist 1 down to the substrate level. With a good etch selectivity between both resists, resist 2 acts as etch mask for resist 1, resulting in inverted features.




**Scheme 3.2** Process flow of dlNIL with the higher etch resistant resist 2 deposited on the mold and resist 1 deposited on the substrate. At a temperature of T > $T_g$, the mold is pressed onto resist 1. Demolding at a temperature below $T_g$ transfers resist 2 to 1. RIE is used to remove the thin residual layer, if at all present. Resist 1 is etched with resist 2 serving as etch mask. With a good etch selectivity the waviness of the substrate is compensated and RIE opens windows in resist 1 to the metal. The metal can be removed by wet etching. Resist is stripped-off by plasma treatment or solvent.

To prove the possibility of combining two resists with dlNIL, poly(methylmethacrylate) (PMMA) was spincoated on a Si substrate and resist mrI-T85 on the OTS-coated mold. Figure 3.6 shows an optical microscope image showing 5 µm wide and spaced lines connected to a 200 µm large pad. The SEM cross section images display the two different resist layers. The green dashed line in Figure 3.6c (a magnification of Figure 3.6b) indicates the interface between the PMMA layer and the mr-IT85 resist. The imprinted mrI-T85 resist was successfully transferred from the mold to the PMMA bottom layer.

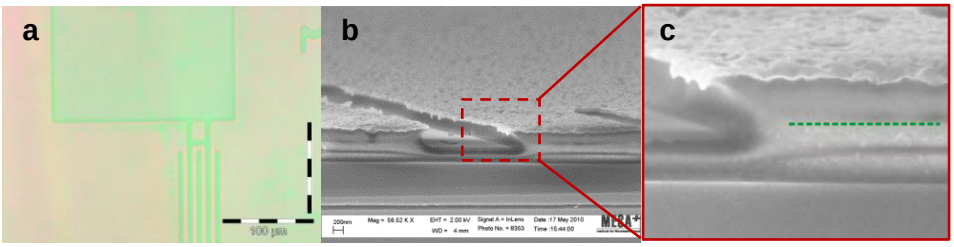



**Figure 3.6** dlNIL-patterned mrI-T85 resist transferred to a PMMA bottom layer deposited on the substrate. (a) Optical microscope image displaying 5 µm wide and spaced interdigitated fingers connected to a 200 µm contact pad. (b, c) SEM images showing the imprinted mrI-T85 resist on top of the PMMA bottom layer on Si with the interface indicated by the green dashed line in (c).

As outlined in Scheme 3.2, the unprotected gold can be wet etched after removal of the residual layer of the top resist (resist 2) and the unprotected resist 1 by RIE. As last step in the process, remaining resist is removed by a strip of in $O_2$ plasma. Metal structures obtained by the presented dlNIL process with two different resists are shown in Figure 3.7.

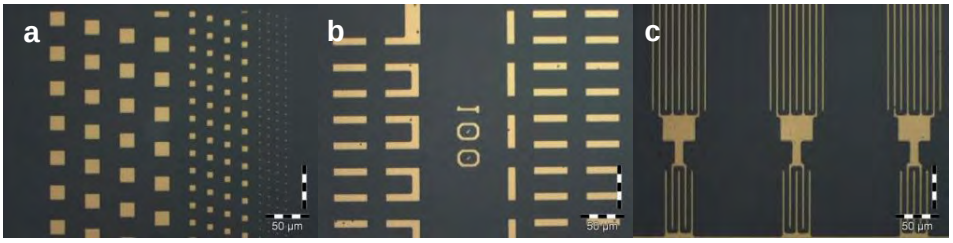



**Figure 3.7** Optical microscopy images of dlNIL-patterned features with an OTS-coated mold on Si after RIE of the residual layer and unprotected PMMA, Au and Ti wet etching and resist strip-off. (a) 1.5 µm, 7 µm and 17 µm wide squares. (b) 40 µm long, 4 µm-wide rectangles and (c) 1.5 µm wide, 5 µm spaced lines connected to a 40 µm pad.

The combination of two resists with dlNIL by applying one to the mold and the other to the substrate is an easy and good working transfer method. The top resist is effectively working as etch mask for the less etch resistant PMMA resist. The here reported technique allows combination of resists not accessible to regular NIL. For instance, undercut structures for lift-off can be fabricated, but also the combination of two heterogeneous resists with different surface energy to control wetting could be thought off.

## 3.3 Conclusions

Resist layers were patterned by three thermal imprinting techniques, namely regular NIL, rNIL and dlNIL, on Si substrates as a model system with an OTS-coated Si mold. With regular NIL, small (<150 μm) features could be patterned, but larger features were not entirely filled, resulting in an inhomogeneous residual layer thickness. On the largest 1.4 mm features the resist in the center of the square feature was removed by RIE before the residual layer on other features could be etched away.

The other two techniques, rNIL and dlNIL, both give access to fully patterned and well transferred resist layers on Si and FOC over an area of 100 mm. With OTS as antisticking layer, resist could be spincoated on top of the Si mold and all protrusions were filled. Of all three studied imprint techniques, only dlNIL has the ability to compensate for imperfectly filled mold protrusions in the imprinting process by resist flowing in from the substrate-deposited resist. This is especially beneficial for very large features and wavy surfaces, for instance foils.

Another unique benefit of dlNIL is the ability to pattern features on wavy foils by combining two resists with different etch properties. With a high enough etch selectivity toward RIE process gases, the inhomogeneous residual layer thickness given in the valleys and hills of the foil can be homogeneously removed without imprint pattern destruction.

A strong benefit of the dlNIL patterning technique is the smart combination of two resists with different properties. This allows extension to many resist combinations for tailored nanostructure fabrication. In this way, dlNIL will enhance the materials versatility of NIL, and contribute to the flourishing field of nano- and microstructuring of functional materials, for example in combination with self-assembly.[26-29]

## 3.4 Experimental Section

### 3.4.1 Materials and Methods

1H,1H,2H,2H-perfluorodecyltrichlorosilane (PFDTS, purity 97%) was purchased from ABCR GmbH & Co.KG. Octadecyltrichlorosilane (OTS, 95% purity) was purchased from Acros Organics. Thermoplastic resists mrI7020E and mrI-T85 were purchased from Microresist Technology GmbH, Berlin. Poly(methyl methacrylate) (PMMA) was purchased from Aldrich and dissolved in Anisole. Teonex Q65a poly(ethylene naphthalate) foil (PEN, 125 μm thick) was purchased from Dupont Teijin. All materials were used as received without further purification.

### 3.4.2 Preparation of Fluorinated Molds

PFDTS was deposited overnight in a desiccator by chemical vapor deposition onto piranha cleaned Si-templates. The subsequent annealing step for 30 min at 100 °C was followed by 10 min ultrasonication in acetone. OTS was applied overnight from a 0.1 mM toluene solution and rinsing with toluene the day after.

### 3.4.3 Resist Deposition

Thermoplastic resist mrI7020E (Microresist Technology GmbH, Berlin) was in all processes spincoated for 5 s at 500 rpm and 20 s at 3000 rpm on the substrate (Si and FOC), followed by a short baking step of 2 min at 120 °C on a hot plate for solvent evaporation. On the Si mold resist is deposited by spincoating 5 s at 500 rpm, 10 s at 1500 rpm, and 15 s at 3000 rpm resulting in a homogeneous layer and fully filled mold. A short baking step of 2 min at 120 °C on a hot plate was performed for solvent evaporation.

### 3.4.4 Thermal Imprinting

Thermal imprinting was performed with the Eitre 6 from Obducat (Malmö, Sweden). The best imprint results were obtained at an imprint temperature of 140 °C under 40 bar pressure for an imprint time of 300 s. Demolding occurred 5 °C below $T_g$, at 55 °C.

### 3.4.5 Residual Layer Removal

The thin residual layer left after imprinting is removed by anisotropic $O_2$ plasma based reactive ion etching. At a chamber pressure of 10 mTorr and 20 sccm $O_2$ the residual layer was removed within 2 min at 20 W.

### 3.4.6 Direct Etching

The with RIE opened windows in the resist layer uncover the Au/Ti metal layer, which is removed by wet etching the 30 nm Au by 10 s exposure to a solution of KI:$I_2$:$H_2O$ 4:1:40 and 15 s exposure of the 5 nm Ti adhesion layer to a 1% HF solution. After being thoroughly rinsed with Milli-Q water and $N_2$ blow drying, resist is stripped off by $O_2$ plasma treatment or by sonication in acetone.

### 3.4.7 Lift-Off

After the residual layer was removed, 5 nm Ti and 30 nm Au were evaporated over the entire substrate. Resist and metal deposited on to the resist were removed by lifting of the resist in acetone, thoroughly rinsing with Milli-Q water and $N_2$ blow drying.

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## Chapter 4

# A Common-Gate Thin-Film Transistor on Poly(ethylene naphthalate) Foil using Step-and-Flash Imprint Lithography

*In this chapter the fabrication of flexible thin-film transistors (TFTs) on poly(ethylene naphthalate) (PEN) foil is reported, with the source-drain layer patterned by step-and-flash imprint lithography (SFIL) as a first step towards fully UV-imprinted TFTs. The semiconductor was deposited by inkjet printing of a blend of TIPS-pentacene/ polystyrene. The bottom-contact, bottom-gate TFTs were fabricated with the foil reversibly glued to a carrier, enhancing the dimensional stability and flatness of the foil to result in a thinner and more homogeneously distributed residual layer thickness. The obtained performance of the TFT devices, showing a mobility of* $\mu = 0.56\ cm^2V^{-1}s^{-1}$ *with an on/off ratio of* $>10^7$ *and near-zero threshold voltage, was found to be in good agreement with similar, photolithographically patterned state-of-the-art devices recently reported in literature. The results presented here show the feasibility of SFIL as a roll-to-roll compatible and downscalable patterning technique on flexible PEN foil for the fabrication of bottom-gate, bottom-contact flexible high-quality TFTs.*

Part of this work has been published in: P. F. Moonen, B. Vratzov, W. T. T. Smaal, G. H. Gelinck, M. Péter, E. R. Meinders, J. Huskens, *Org. Electron.* **2011**, *12*, 2207-2214.

## 4.1 Introduction

The first organic electronic devices developed in the 1980s were the organic photovoltaic cell, the light-emitting diode and the field-effect transistor.[1] The academic and industrial interest in this type of devices has since increased rapidly, especially the technological interest in organic field-effect transistors as potential low-cost and flexible electronic circuitry. Applications in the flexible electronic device area are radio-frequency identification (RFID tags),[2, 3] organic solar cells (OSCs)[4] and active matrices for organic light-emitting displays (OLEDs).[5]

Advanced and flexible organic electronic devices demand high-resolution patterning techniques that, for the sake of low-cost fabrication, can be integrated in high-throughput manufacturing lines such as roll-to-roll (R2R) and roll-to-plate[6] assemblies. The low-cost alternative lithography technique nanoimprint lithography (NIL)[7] provides high-resolution patterning as small as 5 nm[8] combined with short process times. In the original NIL process, developed by Chou *et al.*[9, 10] in 1995, a thermoplastic resist is heated above its glass transition temperature ($T_g$) and embossed by pressing a stamp into it. After cooling down below $T_g$, demolding occurs, leaving a relief pattern on the substrate. Control over pattern replication and residual layer thickness has been improved by the development of UV-based nanoimprint lithography (UV-NIL) in 1996[11] and the further development into step-and-flash lithography (SFIL) by Wilson *et al.*,[12] crosslinking a low-viscosity resist by UV irradiation through a fused silica template. UV-NIL allows room temperature imprinting at low pressures with a good residual layer thickness control, making it (also) an ideal tool for patterning on foil in, for example, a R2R line.

Flexibility is introduced in an organic electronic device by the substrate material, typically being a polyester, polyimide or polycarbonate.[13, 14] Paper has been reported for the fabrication of flexible electronic devices,[15] although the rough surface is limiting the usage of it. Of the polyesters, poly(ethylene terephthalate) (PET) and poly(ethylene naphthalate) (PEN)

are often used[16-18] and are well-studied,[19, 20] combining good mechanical properties and a reasonably high resistance to oxygen and water vapor penetration, making them good candidates for R2R integration. The gas permeability can be further decreased by the deposition of barrier layers such as Ormocer.[21]

The fabrication of flexible electronic devices requires a process with good registration of the involved layers, in particular the registration of the source-drain contacts to the gate layer for TFTs. Flexible organic transistors have been fabricated by photolithographic patterning,[22-26] stamping methods[27] and inkjet printing,[28, 29] all showing different advantages and disadvantages regarding registration, process temperature, feature size and device performance.[1, 28, 30] With conventional printing techniques, typical channel lengths in the range of 10 µm are obtained, limiting the bandwidth to 10 kHz for printable semiconductors with typical mobilities of 0.01 $cm^2V^{-1}s^{-1}$.[31] Fast, sub-micron transistors are, other than with conventional patterning techniques such as photolithography, readily available by NIL, being an intrinsically sub-micron and truly nanometer patterning technique. Organic thin-film transistors have been demonstrated with source-drain contacts defined by thermal NIL on foil[32] and by UV-NIL on glass,[33] both having a photolithographically patterned bottom gate. On PET foil, gate structures have been patterned by UV-NIL, followed by a backside exposure step defining the source-drain contacts in a self-aligned fashion using the previously defined gate as photomask.[31]

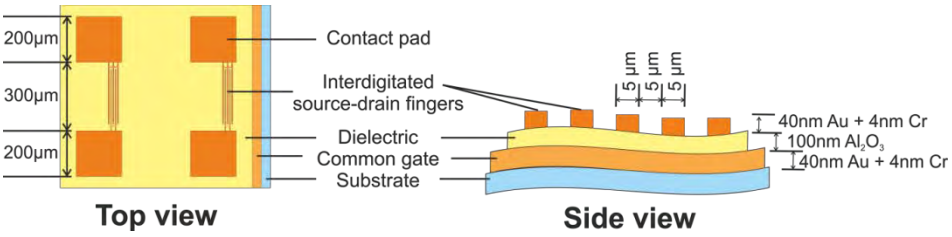
In this study we report common-gate TFTs on flexible PEN foil, in which interdigitated source-drain contacts are defined by SFIL. As such, this work aims to improve earlier reports[31-33] by the combination of electrode design (interdigitated), imprint process (SFIL) and choice of foil substrate (PEN). Future developments will also require patterning of the gate and implementation into R2R to achieve large-area device fabrication. The devices targeted here do not require any alignment step due to the chosen architecture, and can therefore be seen as the first step towards fully patterned, flexible TFTs with all functional layers defined and registered by

UV-NIL. The foil has been reversibly glued to a carrier for improved handling and dimensional stability during the process. SFIL has been chosen as the patterning process not only for its potential for high-resolution patterning, but also and foremost for its potential for implementation into R2R. The semiconductor has been inkjet-printed, and the electronic performance of the fabricated flexible TFTs has been assessed.

## 4.2 Results and Discussion

### 4.2.1 Design and Process Scheme

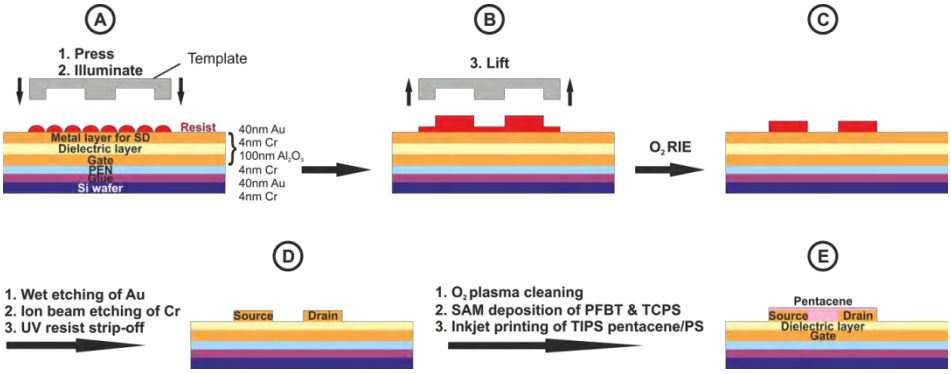
Scheme 4.1 shows a schematic top and side view of the here fabricated flexible thin film transistors (TFTs) in a bottom-contact, bottom and common gate architecture. Source and drain, patterned by SFIL, are made of five interdigitated, 5 µm wide and spaced fingers.




**Scheme 4.1** Schematic top and side view of the TFT architecture. The source-drain layer defined by SFIL is patterned on top of the stack of dielectric and common gate. For each TFT, five interdigitated 5 µm wide and spaced fingers are connected to either the source (three fingers) or drain (two fingers) contact pads, having a width of 200 µm.

Scheme 4.2 shows the process flow for the fabrication of common gate flexible TFTs with an SFIL-defined source-drain layer. Substrates are made of PEN foil, reversibly glued to a carrier (foil-on-carrier; FOC), coated with a metal – insulator – metal (MIM) stack. A UV-curable resist is dropdispensed on the substrate and brought into contact with a UV-transparent template (Scheme 4.2 A). The template is demolded after exposure and curing of the resist with UV light, leaving an inverse replica of the template features on the substrate (Scheme 4.2 B). The remaining residual layer is removed by

reactive ion etching (Scheme 4.2 C). Unprotected Au and Cr are subsequently removed by wet etching and ion beam etching. The remaining resist is stripped off by $O_2$ plasma (Scheme 4.2 D). In the final step, from D to E, first two types of self-assembled monolayers (SAMs), pentafluorobenzenethiol (PFBT) and trichlorophenylsilane (TCPS) (Figure 4.1), are deposited and subsequently the semiconductor, a blend of 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS pentacene) and polystyrene (PS), is deposited by inkjet-printing (Scheme 4.2 E).




**Scheme 4.2** Process flow for the fabrication of common-gate TFTs with imprinted source-drain fingers. In the first step pL amounts of resist are drop-dispensed on the MIM stack-covered foil-on-carrier. (A) The template is pressed into the liquid UV resist and cured for 10 s. (B) After demolding of the template (C) the thin residual layer is removed by $O_2$ RIE. (D) Pattern transfer into the top metal layer is followed by wet etching of the Au in KI:$I_2$:$H_2O$ 4:1:40 and ion beam etching of the 5 nm Cr layer. (E) After the resist is stripped off with $O_2$ plasma, PFBT and TCPS self-assembled monolayers (SAMs) are deposited onto the surface and a blend of TIPS pentacene/PS is inkjet-printed on top of the interdigitated source-drain fingers.

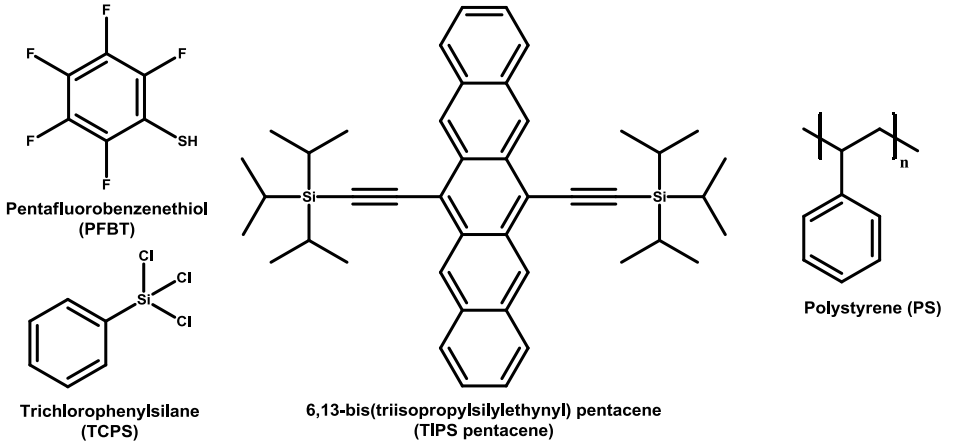



**Figure 4.1** Molecular structures of PFBT and TCPS, deposited as self-assembled monolayers on the Au structures and on the dielectric $Al_2O_3$, respectively, and of the semiconductor blend components TIPS pentacene and PS.

## 4.2.2 Fabrication

The dimensional stability and flatness of the 125 µm thick PEN foils was improved by reversibly gluing them to a carrier (foil-on-carrier; FOC), allowing conformal contact during imprinting and a reduced residual layer thickness. The MIM layer on the FOC was deposited by electron-beam evaporation of subsequently 5 nm Cr, 40 nm Au and 5 nm Cr (common gate), 100 nm $Al_2O_3$ (dielectric), and 5 nm Cr and 40 nm Au as the source-drain layer. Cr was used as an adhesion promoter. The quality of the imprint and the residual layer thickness remaining after imprinting are dominated by the waviness of the fabricated FOC. Significant effort has therefore been devoted to reduce the waviness and bending of the FOCs.

In first attempts, PEN foil was laminated manually, and later on with a lamination tool, onto a glue, followed by thermal curing. The difference in expansion coefficients between the PEN foil, glue and Si wafer led to such a drastic bowing of the FOC (>30 µm) that it could not be taken up by the vacuum chuck in the imprint tool. Contacting of the template on the FOC, homogeneous filling and residual layer formation were not possible due to

the waviness of the foil. In the here developed FOC fabrication technique, the glue was replaced by the thermoplast poly(methyl methacrylate) (PMMA) and spincoated on a Si wafer. The PEN foil was activated by a short plasma treatment and pressed against the PMMA at an elevated temperature of 190°C under 40 bar pressure with a non-patterned Si wafer in an embosser tool (*Eitre*® *6* from Obducat). Surface contour maps of the here developed FOCs (Figure 4.2) were recorded by a contact-free method visualizing the topography of the substrate by measuring the difference in pressure between a measurement and reference $N_2$ stream, being a built-in functionality of the Imprio™ 55. The surface contour maps show the surface waviness to be about 1 µm, uniformity and slightly (~10 µm) elevated edges of the flat embossed, MIM-coated FOCs.

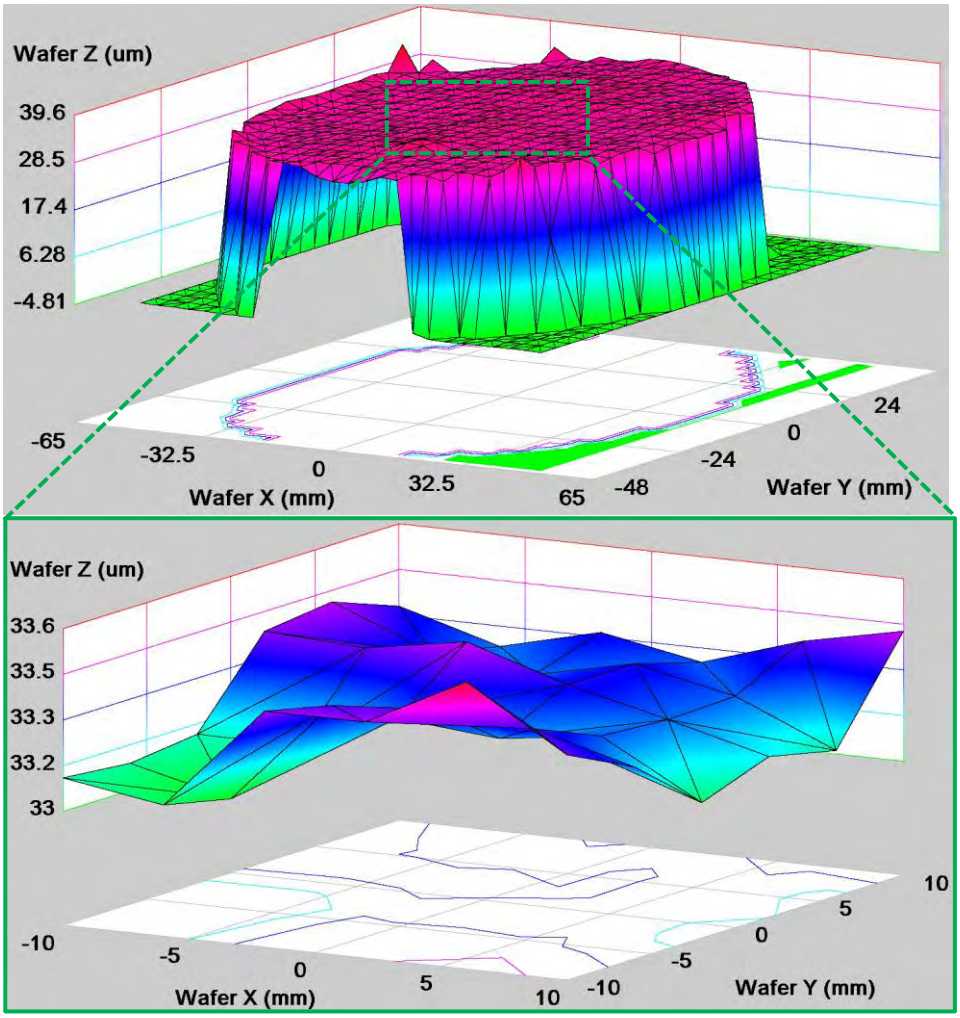



**Figure 4.2** 3D surface contour map of a MIM-coated FOC measured by a contact-free method with $N_2$ pressure as built-in functionality of the Imprio™ 55, showing the surface waviness, uniformity and slightly elevated edges due to bending of the FOC.

The UV-transparent quartz template used as the template for imprinting, contained test features in the dimensional range of 750 nm up to 1.4 mm and the TFT features as shown in Scheme 4.1 on an active area of 15 x 15 $mm^2$ with a depth of 200 nm.

In the first step towards flexible, common-gate TFTs with an SFIL-patterned source-drain layer, a low viscosity, organic, and UV-curable resist (MonoMat™) was field-by-field drop-dispensed in pL amounts onto

the substrate (Scheme 4.2 A, p. 79). The template was brought into contact with the resist droplets under low pressure (2-3 N) at room temperature. Capillary force action pulled the template further down spreading the resist over the active area and filling thereby the structures in the template within 60 s. Broadband UV light was guided through the template curing the resist within 3 s, leaving an inverse replica of the template features on the substrate after demolding (Scheme 4.2 B). An anti-sticking layer (RelMat™) applied to the template before imprinting allowed easy demolding and complete pattern transfer with no residues left on the template. With the field-by-field imprinting technique SFIL, it was possible to imprint the entire FOC (diameter 100 mm) with a throughput of approximately 2 min per field.

The optical microscopy images in Figure 4.3 display 5 µm wide and spaced lines connected to 200 µm square pads directly after imprinting on MIM-coated FOC. The overall residual layer thickness and the filling height of the structures were relatively homogeneous, as can be deduced from the absence of color deviations within the layers. The contrast in color suggests sharply defined edges of the imprinted structures. Pinholes and other filling errors were not observed.

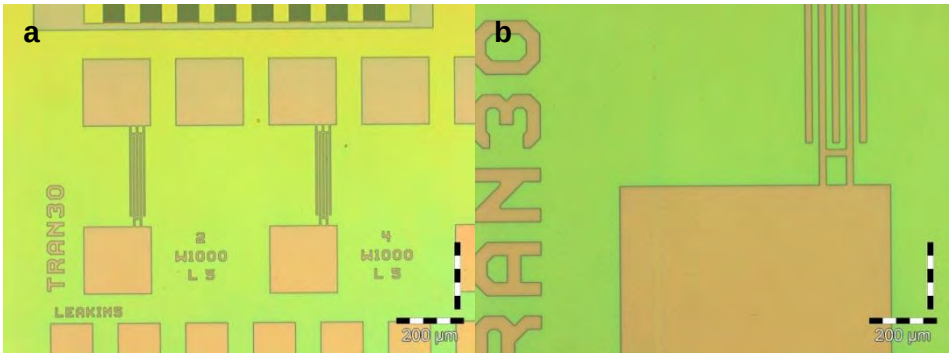



**Figure 4.3** Optical microscopy images of 5 µm wide and spaced interdigitated line structures connected to 200 µm wide contact pads after imprinting (Scheme 4.2B). The substrate is a MIM-coated PEN foil reversibly glued to a carrier.

After imprinting, the residual layer was removed by oxygen-based reactive ion etching ($O_2$ RIE) (Scheme 4.2 C). A residual layer thickness of 80 nm

was determined by profilometry before etching. Especially in the residual layer removal step, the waviness of the FOC plays an important role. Features imprinted on top of a hill of the wave have a thinner residual layer compared to features imprinted in the valley. Removal of the residual layer of features in the wave valleys partially coincides with complete removal of the features on the hills if the feature height is less than the wave height.

The source-drain areas remained covered with resist, allowing selective wet etching of the unprotected Au. The underlying Cr adhesion layer had to be removed by ion beam etching (IBE), as wet etching also lifted the $Al_2O_3$ dielectric layer underneath, due to weak adhesion of the oxide to the underlying gold layer. Improvement of adhesion was attempted by inserting an additional thin layer of Cr on top of the unpatterned gate metal just before oxide deposition. However, the adhesion was not sufficient to withstand the wet etching step. After IBE, the remaining resist was stripped off by $O_2$ plasma (Scheme 4.2 D).

Figure 4.4 shows optical microscopy images of the features after residual layer removal, wet etching of the Au, dry etching of the Cr layer, and resist strip-off. The bright yellow color indicates the Au features on the (orange colored) $Al_2O_3$ dielectric layer. The features appear sharply defined and no pinholes were observed, as deduced from the absence of bright spots in the closed orange layer.

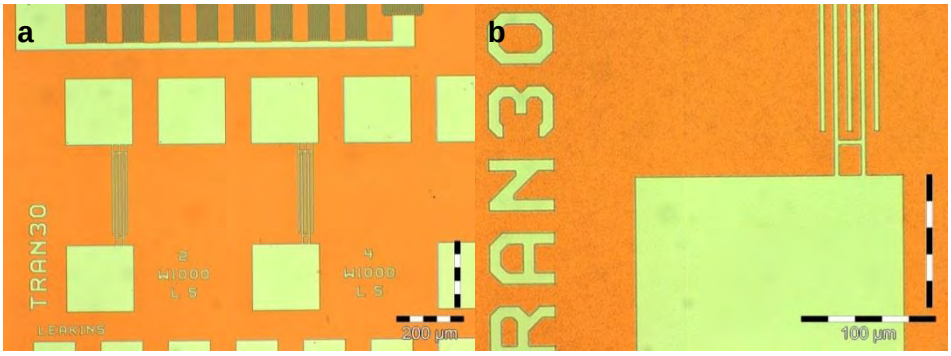



**Figure 4.4** Optical microscopy images of 5 µm wide and spaced interdigitated source-drain fingers connected to 200 µm wide contact pads after imprinting, residual layer removal, wet etching of the unprotected Au and dry etching of Cr and resist strip-off (Scheme 2D). The substrate is a MIM-coated PEN foil reversibly glued to a carrier.

As the TFT was made in a bottom-contact, bottom-gate architecture, the final layer added to the device was the organic semiconductor. A PFBT SAM was deposited from ethanol solution on all gold contacts to modify the charge injection.[34] TCPS was deposited by vapor deposition on all oxide surfaces to reduce electron trapping. SAMs are known to improve the molecular order of the deposited semiconductor.[35] A blend of TIPS pentacene:PS in a 2:1 w/w ratio, was inkjet-printed at a substrate temperature of 70°C from tetraline solution onto the interdigitated source-drain fingers, leading to TIPS pentacene crystals grown from the edge to the center of the inkjet-printed droplets.[36]

Figure 4.5a shows an optical microscopy image of inkjet-printed TIPS pentacene/PS on the interdigitated source-drain fingers patterned by SFIL. Accurate control of the dispensing unit allowed the deposition of one drop of semiconductor on each of the four TFTs. A microscope image taken with cross polarizers shows the crystal orientation of the birefringent TIPS pentacene crystals, pointing to the center of the drop (Figure 4.5b).

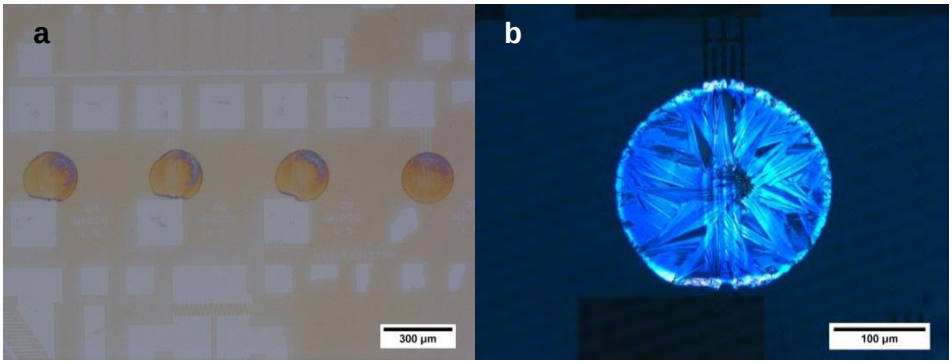



**Figure 4.5** Optical microscopy images of bottom contact, bottom gate TFTs with SFIL-patterned source-drain fingers on a MIM-covered FOC with inkjet-printed TIPS pentacene/PS crystals after SAM deposition of PFBT and TCPS (Scheme 4.2 E). (a) One drop of TIPS pentacene/PS inkjet-printed on each of the four interdigitated 5 µm wide and spaced source-drain fingers. (b) Crossed polarizer optical microscopy image of one drop of TIPS pentacene/PS inkjet printed on the source-drain fingers showing a crystal growth from the edge to the center.

The high resolution SEM images in Figure 4.6 show the final TFTs after semiconductor deposition, displaying a line edge roughness (LER) of about

70 nm caused by the short (10 s) wet etching of the gold. Any LER introduced by imprinting, representing an exact replica of the LER of the template, is negligibly small in comparison to the LER caused by wet etching of the gold.

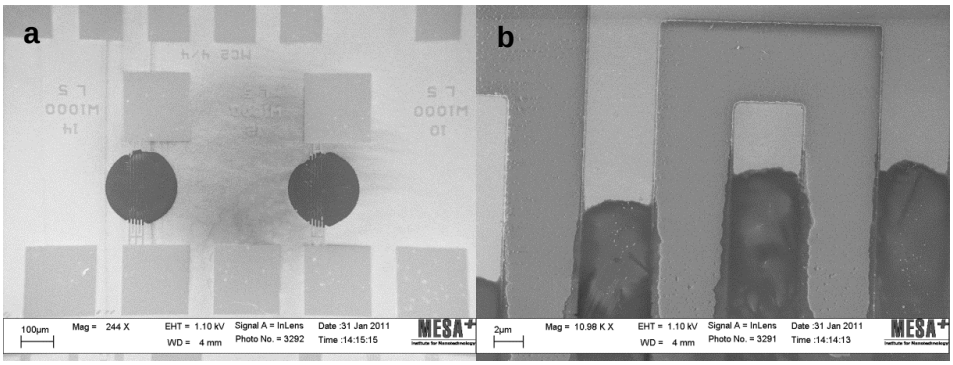



**Figure 4.6** High resolution SEM images after semiconductor deposition of (a) two TFTs, and (b) part of the source drain fingers displaying a line edge roughness of ~70 nm caused by wet etching.

## 4.2.3 Electrical Characterization

Electrical characterization of the SFIL-patterned flexible TFTs was performed in a non-illuminated glove box under $N_2$ atmosphere. The contact to the common gate was established by penetrating the dielectric layer with one of the probe station needles. The source and drain contact pads were each gently contacted with another probe needle. The gate voltage was varied from 5 V to -5 V in a double scan and the bias over source and drain ($V_{DS}$) held at -1 V and -5 V. The transfer and output characteristics of the best out of six transistors with a channel length L= 5 µm and a channel width W= 766 µm arranged in a comb structure are given in Figure 4.7. The transfer characteristics of five more transistors are shown in Figure 4.8 to give an insight in the spread of the samples.

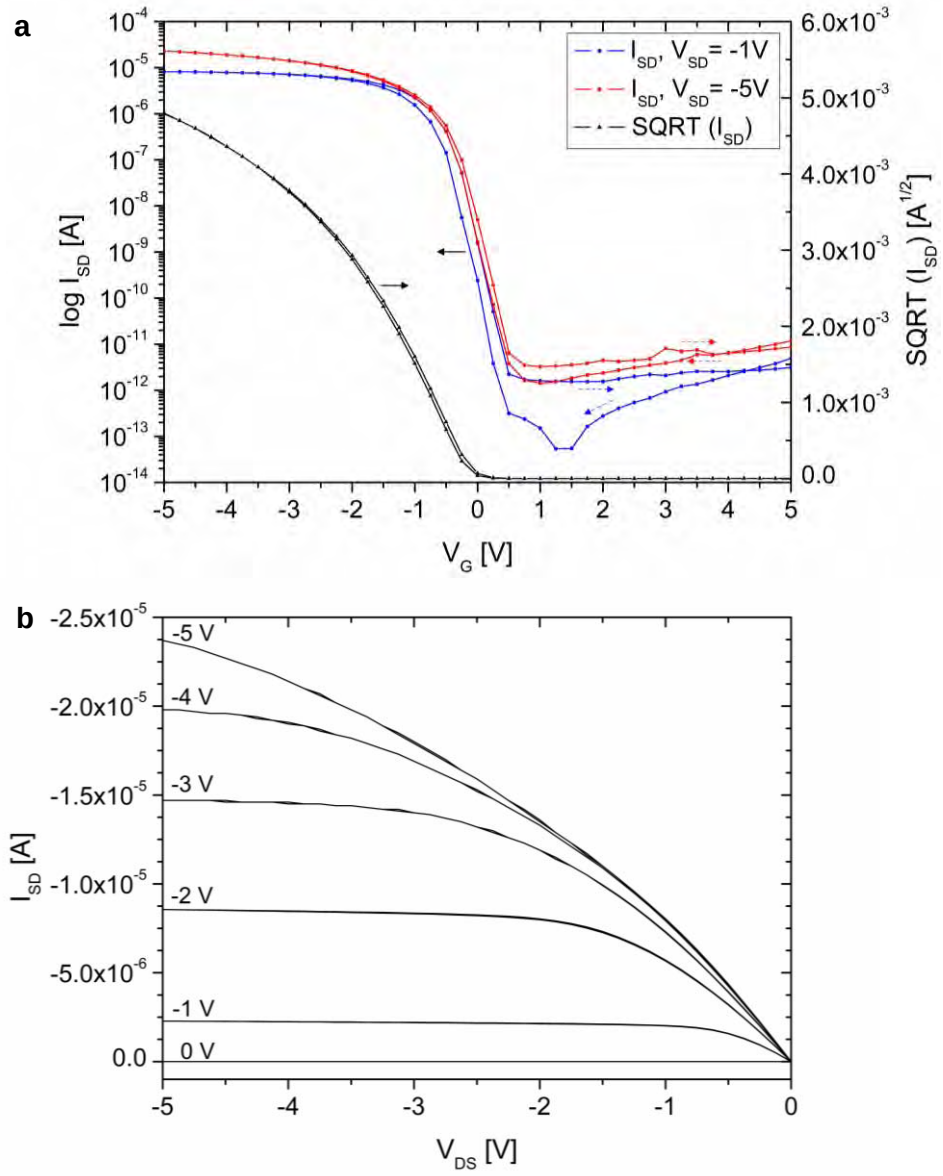



**Figure 4.7** (a) Transfer characteristics of an SFIL-patterned TFT in a bottom contact, bottom gate architecture. Channel length and width are 5 and 766 μm, respectively. A 100 nm thick $Al_2O_3$ layer served as the gate dielectric, and a blend of TIPS pentacene/PS as the semiconductor. The dashed arrows indicate the sweep direction (gate swept from +5V to -5V to +5V). (b) Output characteristics of the same transistor. $V_G$ was varied between 0 and -5V at a step of -1V.

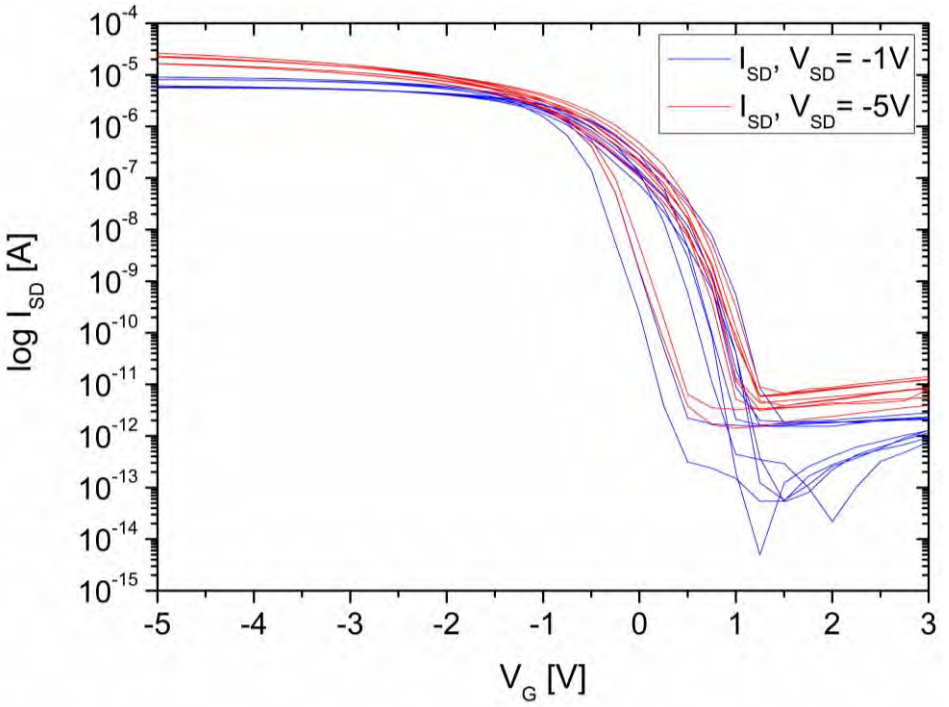



**Figure 4.8** Transfer characteristics of five SFIL-patterned TFTs in bottom contact, bottom gate architecture. Channel length and width are 5 and 1000 µm, respectively. A 100 nm thick $Al_2O_3$ layer served as the gate dielectric, and a blend of TIPS pentacene/PS as the semiconductor.

From the semi-logarithmic plot (log $I_{SD}$ vs. $V_G$) for the best TFT (Figure 4.7a), a sub-threshold swing (SS) of 190 mV/dec, an on/off ratio of $2x10^7$, and a switch-on voltage of $V_{SO}$= 0.4 V were obtained. The switch-on voltage was taken as the gate voltage at which the drain current is one order of magnitude higher than the off-current $I_{off}$.[33] From the plot of the square root of $I_{SD}$ vs. $V_G$, a gate-dependent mobility of $\mu_{SAT}$= 0.56 $cm^2V^{-1}s^{-1}$ at $V_G$= -0.75 V (average over all six transistors: $\mu_{SAT}$= 0.37 ± 0.08 $cm^2V^{-1}s^{-1}$) and a near-zero threshold voltage of $V_{th}$= -0.1 V were determined. The here obtained TFT values are in good agreement with literature data measured under similar conditions. The averaged mobility obtained for photolithographically defined bottom-contact, bottom-gate TFTs on poly(ethylene terephthalate) foil with a (sputtered) $Al_2O_3$ gate dielectric and inkjet printed TIPS pentacene on SAM-treated contacts and a channel width over length of 1000 µm/5 µm is µ= 0.22 ± 0.03 $cm^2V^{-1}s^{-1}$.[37] The

mobility obtained here using imprinting is slightly higher, possibly caused by an improved LER or cleaner interfaces. Previously reported TFTs with TIPS pentacene/PS (67wt%) blend inkjet printed on photolithographically patterned Au source-drain electrodes on highly doped $n^{++}$ Si wafers with 140 nm thermally grown $SiO_2$, showed an improved mobility of $\mu_{SAT} \approx 0.73\ cm^2V^{-1}s^{-1} \pm 23\%$ for a channel length of 5 µm.[36] The on/off current and the threshold voltage of these non-flexible TFTs are very similar to the here obtained values. Only a steeper SS of 67 mV/dec was obtained. A steep SS and low $V_{th}$, are usually taken as evidence for a high-quality gate dielectric - semiconductor interface with few charge trapping centers.[36] The higher mobility reported for the non-flexible TFTs is believed to be due to the higher quality thermally grown gate dielectric, compared to the e-gun evaporated $SiO_2$ deposited on the here presented SFIL-patterned flexible transistors. The results shown here confirm that high-quality TFT devices can be made using NIL which holds promise for facile R2R production and further extension to sub-micron and nanoscale feature sizes.

## 4.3 Conclusions

In this chapter the feasibility of SFIL as a patterning technique on flexible PEN foil is shown for the fabrication of bottom-gate (common) and bottom-contact flexible TFTs. Using this R2R-compatible and downscalable technique in combination with inkjet printing, excellent flexible TFTs with a performance comparable with state-of-the-art devices fabricated by optical photolithographic patterning[36-38] were obtained.

Future plans concern the fabrication of flexible, patterned-gate TFTs with all functional layers patterned by the room temperature, low pressure and high precision technique SFIL. The channel length of the flexible, all-patterned TFTs will also be reduced to the sub-micrometer regime. Downscaling into the sub-micrometer regime will result in an increased impact of the LER on the performance and dimensions of the device. Wet

etching of the gold is at this stage the main factor introducing LER. Therefore, an etch process with an improved LER control, such as ion beam etching, should be introduced. The final flexible TFT fabrication process is envisioned to be R2R imprinting. R2R processing requires a patterning process independent of any alignment step, as the critical source-drain to gate overlay cannot be registered precise enough. Therefore, efforts are undertaken toward the development of a self-aligned imprinting process, implementing the fabrication lessons learned here. As soon as device layout, process parameters and R2R implementation have been achieved, other performance issues such as mechanical stability and environmental stability will be addressed as well.

## 4.4 Experimental Section

### 4.4.1 Materials and Methods

Imprint resist MonoMat and anti-sticking layer RELMAT were purchased from Molecular Imprints, Inc. Teonex® Q65a poly(ethylene naphthalate) foil (PEN, 125 μm thick) was purchased from Dupont Teijin. 6,13-Bis(triisopropyl-silylethynyl) pentacene (TIPS pentacene) was synthesized according to literature.[39] Polystyrene (PS) $M_w \approx$ 9.58 kDa ($M_n$= 9.32 kDa, PDI= 1.03) was purchased from Fluka. 1,2,3,4-Tetrahydro-naphthalene (tetraline) was purchased from Merck.

### 4.4.2 Foil-on-Carrier (FOC)

FOCs were made by laminating the PEN foil to a glue, previously deposited on a double-side polished wafer. As glue, a 6 wt% solution of poly(methyl methacrylate) ($M_w$= ~38 kDa) dissolved in toluene, both purchased from Aldrich, was spincoated on a double-side polished wafer. The stack of glue-coated wafer, activated foil and a double-side polished (unpatterned) wafer with an 1H,1H,2H,2H-perfluorodecyltrichlorosilane anti-sticking layer applied by chemical vapor deposition, were loaded in an embossing tool

(Eitre® 6 from Obducat, Malmö, Sweden). The foil was glued to the wafer by heating up the stack to 190°C under 40 bar pressure for 500 s. The top wafer (with anti-sticking layer) was demolded at a temperature of 95°C from the finished FOC. The PEN foil could be delaminated again from the carrier by heating to a temperature of 150°C or by dissolving the PMMA in acetone.

The MIM layer was deposited on the FOC by e-gun evaporation of subsequently 5 nm Cr, 30 nm Au and 5 nm Cr forming the common gate, 100 nm $Al_2O_3$ as gate dielectric, and 5 nm Cr and 30 nm Au as source-drain metal.

### 4.4.3 Step-and-Flash Imprint Lithography (SFIL)

The UV-transparent quartz template used for the experiments was fabricated by standard e-beam lithography and RIE techniques. The template contained, on an active area of 15 x 15 $mm^2$, test features in the dimensional range of 750 nm up to 1.4 mm and the TFT features as shown in Scheme 4.1 with a depth of 200 nm.

SFIL was performed with an Imprio 55 tool from Molecular Imprints, Inc. The imprints were carried out at room temperature and under a force of 3 N. For improved adhesion of the imprint resist (MonoMat™), the Au surface of the FOC was activated just before use by a short $O_2$ plasma treatment of 5 min at 300 W and 18 sccm $O_2$ (Apparatus Tepla 300E). MonoMat™, after field by field drop dispensing on the substrate, filled the template within 60 sec and was cured through the backside of the template for 3 s with broad band UV light (exposure dose of 80 $mJ/cm^2$ and $\lambda$= 230-360 nm).

### 4.4.4 Residual Layer Removal

The thin residual layer left after imprinting was removed by anisotropic $O_2$ plasma based reactive ion etching in a homebuilt tool (Etske). At a chamber

pressure of 10 mTorr and 20 sccm $O_2$ the residual layer was removed within 1 min at 20 W.

### 4.4.5 Direct Etching

RIE opened windows in the resist layer which uncovered the Au/Cr metal layer. The 30 nm Au layer was removed by 10 s wet etching in a solution of KI:$I_2$:$H_2O$ 4:1:400. The 5 nm Cr adhesion layer was removed by Ar ion beam etching with an Oxford Ionfab 300, removing the Cr layer within 3 min, controlled by an endpoint detection system.

### 4.4.6 Resist Strip-Off

Remaining resist was stripped off in a Tepla 300E, by generation of an 300 W $O_2$ plasma (18 sccm) for 10 min.

### 4.4.7 Self-Assembled Monolayers

PFBT was deposited by 15 min exposure to a 10 mM PFBT solution in ethanol, followed by rinsing with ethanol and $N_2$ blow drying. $N_2$ was utilized as carrier gas bubbling through TCPS in a closed chamber at atmospheric pressure for 15 min to deposit TCPS on all oxide areas. The substrates were baked 2 min at 100°C on a hot plate after flushing the chamber with $N_2$ to remove the side product (hydrochloric acid) of the condensation reaction.

### 4.4.8 Semiconductor Deposition

An inkjet printing setup with a high-precision vertical translation stage and a Microfab glass nozzle (type MJ-ATP-01-50-DLC, 50 µm orifice diameter) was used to print the blend of TIPS pentacene (20 mg/ml) : PS (10 mg/ml) in a blending ratio of 2:1. Droplets with a volume of 50 pL were jetted on demand, onto transistor substrates kept at a temperature of 70°C. All printing experiments were performed in ambient cleanroom conditions.[36]

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## Chapter 5

# Thin-Film Transistors with (Sub)Micron Channel Lengths on Si and Poly(ethylene naphthalate) Foil Exclusively Patterned by UV Nano-imprint Lithography

*In this chapter, a multistep imprinting process is presented for the fabrication of a flexible bottom-contact, bottom-gate thin-film transistor (TFT) on poly(ethylene naphthalate) (PEN) foil by patterning all layers of the metal-insulator-metal stack by UV nanoimprint lithography (UV NIL). The flexible TFTs were fabricated on a planarization layer, patterned in a novel way using UV NIL, on a foil reversibly glued to a Si carrier. This planarization step enhances the dimensional stability and flatness of the foil and thus results in a thinner and more homogeneous residual layer. The fabricated TFTs have been electrically characterized as demonstrators of the here developed fully UV NIL-based patterning process on PEN foil, and compared to TFTs made on Si with the same process. TFTs with channel lengths from 5 μm down to 250 nm have been fabricated on Si and PEN foil, showing channel length-dependent charge carrier mobilities, μ, in the range of 0.06 - 0.92 $cm^2V^{-1}s^{-1}$ on Si and of 0.16 - 0.56 $cm^2V^{-1}s^{-1}$ on PEN foil.*

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## 5.1 Introduction

In a world following the ever demanding decrease of feature sizes for the fabrication of faster electronic circuits and devices according to Moore's law,[1] research and development of tools allowing reproducible patterning at an ever decreasing scale gain increasing attention. On the other hand, electronics manufacturers focus on reducing fabrication costs and on the addition of device functionalities. Of great interest in this direction are organic plastic electronics, allowing potentially low-cost fabrication, in combination with the introduction of light-weight, flexibility and transparency, in high throughput roll-to-roll (R2R) or roll-to-plate[2] manufacturing lines. Transparent, bendable and even rollable flexible electronic devices such as organic light-emitting diode (OLED)-based displays,[3] radio-frequency identification (RFID) tags,[4-5] and organic solar cells (OSCs)[6] are being pursued. However, flexible electronic devices face new challenges, not necessarily originating from the small dimensions of the device, but from deformations and the dimensional instability of the substrate.[7]

In combination with R2R manufacturing for low-cost fabrication of plastic electronics, the high-resolution[8-9] patterning technique nanoimprint lithography (NIL) is an excellent candidate. The classical thermal NIL[10-12] has been further developed into UV-based NIL,[13] and as repetitive technique into step-and stamp[14] and step-and-flash imprint lithography (SFIL),[15] allowing better control over the residual layer thickness and throughput, by crosslinking a low-viscosity resist by UV irradiation through a fused silica template. Flexible organic thin-film transistors (OTFTs) have been fabricated by photolithographic patterning,[7, 16-19] stamping methods[20] and inkjet printing,[21-24] all showing different advantages and disadvantages regarding layer registration, process temperature, feature sizes and device performance.[21, 25-26] With conventional printing techniques, typical channel lengths on the order of 10 µm are obtained, limiting the bandwidth to 10 kHz for printable semiconductors with typical mobilities of 0.01 $cm^2V^{-1}s^{-1}$.[27] Fast, sub-micron transistors are, other than

with conventional patterning techniques such as photolithography, readily available by NIL, being an intrinsically sub-micron and truly nanometer patterning technique.

In literature, TFTs have been reported with source-drain features patterned by UV NIL on flexible foil in a common gate architecture (Chapter 4) and on glass with a photolithographically defined gate.[28] TFTs with the source-drain features patterned by thermal NIL and a photolithographically defined gate have also been reported.[29] Common gate TFTs cannot be addressed individually and suffer from parasitic effects (capacitances, resistances, inductances). Multilayered, patterned gate TFTs on the other hand, can be addressed individually in an array and show an improved performance. Fabricating a multilayer electronic device requires a good layer registration and overlay accuracy. Patterning on flexible and wavy foils, showing in-plane instabilities and a high sensitivity to thermal as well as pressure changes, remains a big challenge. With the low-cost and sub-micron patterning technique UV NIL, precise nano- to sub-micron alignment are just as important as critical control over the residual layer thickness (RLT) for the performance of a layer-by-layer fabricated, complex electronic device such as a bottom-contact, bottom-gate TFT. To our knowledge, a fully UV NIL-patterned TFT on foil has not been reported to date.

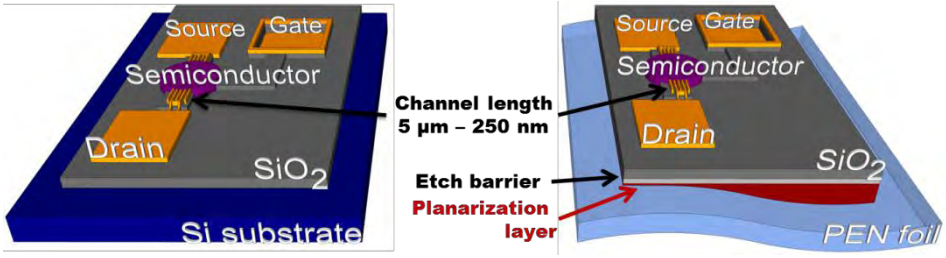
Here we report a method for fabricating bottom-contact, bottom-gate TFTs on Si and on flexible PEN foil with all functional layers patterned with the fast and low-cost patterning strategy SFIL. The complexity of the device layout is strongly increased with respect to the earlier reported flexible, common-gate TFTs (Chapter 4) in which only the source-drain layer was patterned by SFIL. In this multilayered device the gate, source-drain and gate-via are patterned by SFIL, showing a good layer definition and registration accuracy, even on the dimensionally instable, flexible PEN foils. The flexible TFTs were fabricated with the foil reversibly glued to a carrier (foil-on-carrier; FOC), enhancing the dimensional stability and flatness of the foil to result in a thinner and more homogeneously distributed RLT.

Exact alignment of gate and source-drain on the foil requires an even further improved control over the residual layer, which is targeted here by field-by-field planarization. The transfer and output characteristics of the here fabricated flexible TFTs will be compared with TFTs fabricated on Si with the identical, fully SFIL-based process.

## 5.2 Results and Discussion

### 5.2.1 Design and Process Scheme

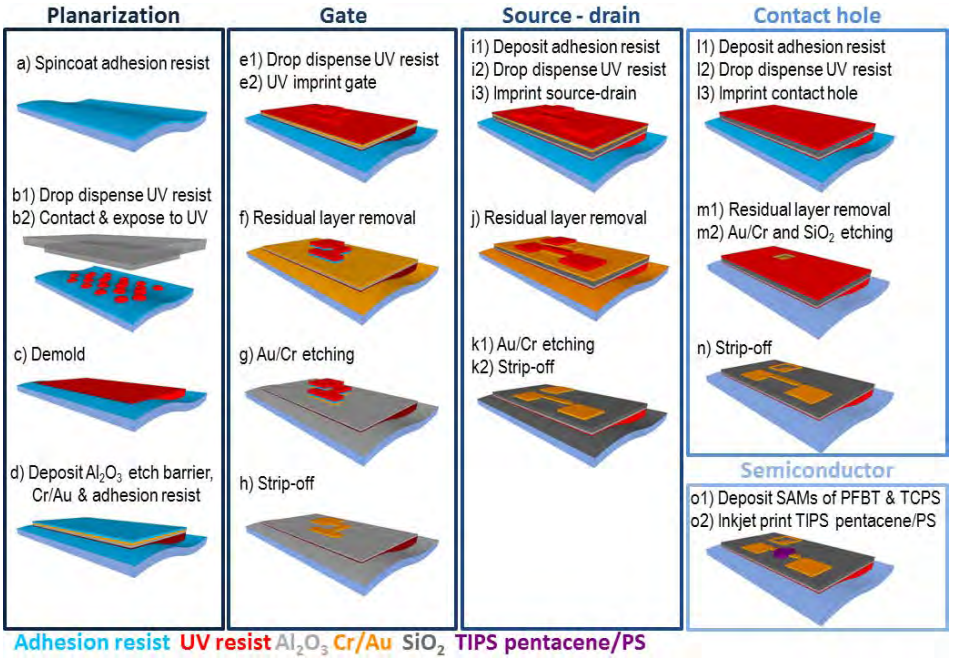
Scheme 5.1 shows a schematic three-dimensional view of the here fabricated TFTs on Si and foil in a bottom-contact, bottom-gate architecture. The gate, source-drain and contact hole features are patterned by SFIL, while the semiconductor is deposited by inkjet printing. In case of patterning on foil, also the planarization layer is patterned by SFIL. The 200 x 200 µm² contact pads of the source and drain are connected to three or two 5 µm-wide interdigitated fingers separated by a space of 5 µm down to 250 nm, representing the channel length.




**Scheme 5.1** Schematic view of the here fabricated bottom-contact, bottom-gate TFTs on (a) Si and (b) PEN foil. Gate, source-drain and contact hole have been subsequently patterned by SFIL. For the flexible TFTs, a planarization layer of 25 x 25 mm² has been formed by imprinting, and an oxide etch barrier has been deposited before imprinting the gate. The semiconductor has been inkjet-printed on the five 5-micron wide, interdigitated source-drain fingers, with channel lengths of 5 µm down to 250 nm. The square contact pads are 200 x 200 µm².

Scheme 5.2 shows the here developed multistep UV imprinting process on PEN foil, with a flexible TFT as the resulting demonstrator. The process scheme for the TFT on Si is the same, except for the planarization layer. For

better understanding, the carrier to which the foil has been reversibly glued is not drawn in the scheme. In the first step, the planarization layer is formed on the wavy PEN foil. The UV resist is drop-dispensed on adhesion resist-coated (DUV30J) PEN, followed by contacting with a UV transparent, non-patterned template (Scheme 5.2b). After UV exposure, the template is demolded and a planarized plateau of 25 x 25 $mm^2$ remains (Scheme 5.2c). An alumina etch barrier, Cr and Au for the gate layer, and adhesion resist DUV30J are subsequently deposited (Scheme 5.2d). To pattern the gate, the UV resist is drop-dispensed on the adhesion resist (Scheme 5.2e1) followed by contacting with the gate template. After UV exposure, an inverse replica of the gate template features remain on the foil (Scheme 5.2e2). The residual layer is removed by oxygen-based anisotropic reactive ion etching ($O_2$ RIE) (Scheme 5.2f), and unprotected Au and Cr are removed by ion beam etching (IBE) (Scheme 5.2g). The remaining resist is stripped off in $O_2$ RIE, leaving the patterned gate on the substrate (Scheme 5.2h). The source-drain layer is patterned in a similar fashion. First, the dielectric (150 nm $SiO_2$), Cr and Au for the source-drain layer, and adhesion resist are deposited. The source-drain features are patterned by exposure of drop-dispensed UV resist with the source-drain template aligned to the previously deposited gate layer (Scheme 5.2i1-3). Residual layer removal (Scheme 5.2j) is followed by IBE and resist strip-off, resulting in a patterned source-drain layer (Scheme 5.2k). Contact holes are made through the dielectric by imprinting the contact hole features in UV resist, with the contact-hole template aligned to the previously patterned gate layer (Scheme 5.2l). Residual layer removal and IBE of deposited Au, Cr and $SiO_2$ (Scheme 5.2m) are followed by resist strip-off, resulting in direct access to the gate contact pad (Scheme 5.2n). The semiconductor is deposited as the last processing step. Two self-assembled monolayers (SAMs), of pentafluorobenzenethiol (PFBT) and trichlorophenylsilane (TCPS), are applied (Scheme 5.2o1) prior to deposition of the semiconductor by inkjet-printing of a blend of 6,13-bis(triisopropylsilyl-ethynyl) pentacene (TIPS pentacene) and polystyrene (PS)[30] (Scheme 5.2o2).




**Scheme 5.2** Process flow for the fabrication of flexible TFTs with the planarization, gate, source-drain and contact hole layers patterned by SFIL. The semiconductor is patterned by inkjet printing. TFTs on Si are made in a similar fashion, leaving out the planarization layer.

## 5.2.2 Fabrication

In the fabrication process of the flexible TFTs, the dimensionally instable foil plays a crucial role. A wavy substrate results during the imprinting process in an inhomogeneous residual layer, being thicker in the wave valleys and thinner on the wave hills. Removing the residual layer of features in the wave valleys partially coincides with complete removal of the features on the hills if the feature height is less than the wave height. Reversible lamination of the foil on a Si carrier improved handling and reduced the overall waviness to <1 µm with a total wafer bowing of <10 µm. FOC bowing is induced by a difference in coefficients of thermal expansion between the foil, glue and Si wafer,[31] and has been observed for planarization materials and glues tested for reversible gluing of the foil to the carrier.[7, 15, 32] An earlier reported FOC fabrication process (Chapter 4),

made by thermal flat-embossing of the foil on a poly(methylmethacrylate) (PMMA)-coated Si wafer with a non-patterned Si wafer as the mold, was replaced by a FOC made by reversible lamination of a thinner and therefore less stress-inducing 25 µm PEN foil. However, the substrate was still found to be insufficiently flat, with an overall waviness of ~1.0 µm, to pattern all three layers by SFIL due to a too inhomogeneous RLT.

Therefore, we developed a fast and simple method for field-by-field planarization of wavy substrates. With SFIL, a 25 x 25 mm² flat area was imprinted on the wavy substrate by pressing, at room temperature under low pressure, a non-patterned template against the foil. The self-leveling capability of the template during imprinting, caused by capillary forces pulling down the template against the foil, resulted in an imprinted, flat plateau on the foil surface. Surface contour maps recorded before (Figure 5.1a) and after (Figure 5.1b) imprint planarization of the same area on the FOC show the decrease of the surface waviness from 700 nm in the non-planarized state to 260 nm on the planarized foil over an area of 12 x 12 mm². Planarization provides a sufficiently flat surface to obtain a thin and homogeneous residual layer, thus allowing multiple imprint steps.

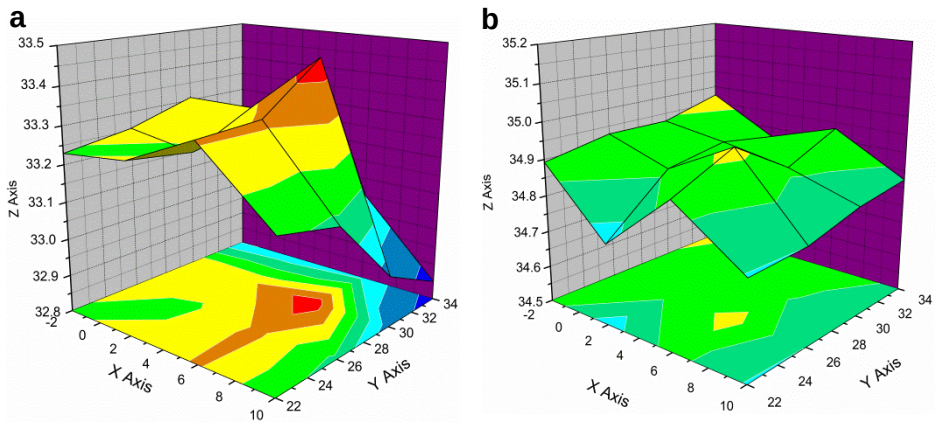



**Figure 5.1** Surface contour maps of a FOC showing a surface waviness over an area of 12x12 mm² of (a) 700 nm without and (b) 260 nm with an imprinted planarization layer. The z-range in both maps is 700 nm.

The set of three UV-transparent fused silica templates used here for subsequent imprinting of the gate, source-drain and contact hole layers,

contained features in the dimensional range of 100 nm up to 750 µm with a depth of 300 nm on an active area of 11 x 11 $mm^2$.

Before patterning the first layer of the TFT on the FOC, an etch stop of 50 nm $Al_2O_3$ was evaporated on the planarization layer, to protect the planarization layer made of imprint resist from being etched during gate processing or resist strip-off. Without etch stop, a higher current leakage or even shorts between the source-drain and gate layer were observed and some TFTs burned through after multiple I/V measurements right at the edge of the gate. With an etched planarization layer, the source-drain fingers had to cover a step height of about 150 nm, which is 100 nm more than initially designed (Figure 5.2a). The source-drain fingers thus became very thin at this large step and heated up quickly due to resistance, while the source-drain contact pad was very close to the gate causing a high leakage current. Introduction of the oxide etch stop resulted in a step height of only 50 nm (Figure 5.2b), whereafter no shorts or burned TFTs were observed anymore.

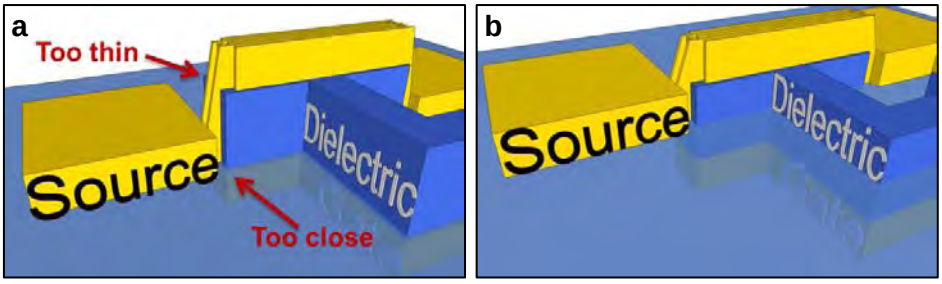



**Figure 5.2** Schematic 3D representation of the layout of the bottom-gate TFT (a) without and (b) with an etch barrier, protecting the planarization from being etched. With etched planarization layer (a), the source-drain fingers are thinned down and therefore vulnerable to overheating due to increased resistance and the source (or drain) contact pad is at close proximity to the gate, leading to an increased gate leakage. With an etch stop (b), source-drain and gate are well separated and the source-drain fingers are thick enough to allow the current to flow.

For the gate layer itself, 3 nm Cr adhesion metal and 47 nm Au were deposited by e-gun evaporation on the etch stop layer. Sputtering was not an option, as it would heat up the foil too strongly. The SFIL patterning process, being the same for all three layers, will be exemplarily explained

for the gate layer in the following lines. Where applicable, differences in the patterning process between the three layers will be noted.

As adhesion promoter for the imprint resist, a 60 nm thick layer of DUV30J was spincoated on the entire sample. A low-viscosity, organic, and UV-curable resist (MonoMat™) was field-by-field drop-dispensed in pL amounts onto the substrate. The template was brought into contact with the resist droplets under low pressure (2-3 N) at room temperature. Capillary force action pulled the template further down spreading the resist over the active area and filling thereby the structures in the template within 60 s. Broadband UV light was guided through the template curing the resist within 3 s, leaving an inverse replica of the template features on the substrate after demolding. An anti-sticking layer (RelMat™) applied to the template before imprinting allowed easy demolding and complete pattern transfer with no residues remaining on the template. The residual layer of approximately 80 nm, recorded by profilometry, was removed by anisotropic oxygen-based reactive ion etching ($O_2$ RIE) after imprinting. The gate (or source-drain) features remained covered with resist, allowing selective removal of the unprotected Au and Cr within 4 min by Ar ion beam etching (IBE). Wet etching of the metal layers was not an option, especially for the sub-micron features, as it created a line edge roughness (LER) of around 100 nm and induced pattern destruction by partial lifting or entire removal of the features. In case of patterning the source-drain layer, the underlying dielectric was also negatively affected by wet etching, predominantly by oxide removal. The third imprinted layer of the flexible TFT left a protective resist mask over the entire sample, except for a window of 180 x 180 $\mu m^2$ exactly above the gate contact pad. The residual layer was removed by $O_2$ RIE and the underlying metals and dielectric were removed by ion beam etching within 10 min, creating a contact hole to the gate. After pattern transfer of the imprinted features into the underlying layer by ion beam etching, the remaining resist was stripped off.

The different stages of the multilayer fabrication of the flexible TFT by UV NIL on foil are shown in Figure 5.3. The first patterned layer was the 70 µm

wide gate (Figure 5.3a-b), followed by the source-drain layer with source-drain fingers separated by a line spacing of 5 μm down to 200 nm. The smallest channel lengths fabricated on PEN foil, separating the 5 μm wide source-drain fingers, were 500 nm and 200 nm (Figure 5.3c-f). As third and last patterned layer, contact holes of 180 x 180 $\mu m^2$ were made through the dielectric (Figure 5.3g-h).

The images in Figure 5.3 show that all layers of our multilayer device have been successfully patterned on PEN foil with the above described patterning strategy. The subsequently deposited and patterned layers adhered well to each other and to the substrate. The patterned features exhibit sharp edges and rectangular corners, from the largest channel dimensions of 5 μm down to the smallest 200 nm channels. A small line edge roughness of around 40 nm (Figure 5.3d) is visible, dominated by the ion beam etching process to remove unmasked metal. Wet etching would have created, as reported above, a LER of ~100 nm. Alignment of the gate to the source-drain layer was achieved by overlay of two gratings with a difference in line periodicity of 25 nm creating a moiré interference pattern. An alignment accuracy of the source-drain to the gate of 25 - 200 nm on Si and 50-300 nm on FOC has thus been obtained. The overlay of the source-drain fingers to the gate was made asymmetric on purpose (Figure 5.3g-h), allowing the gate to control a larger area of the inkjet-printed semiconductor during device operation.

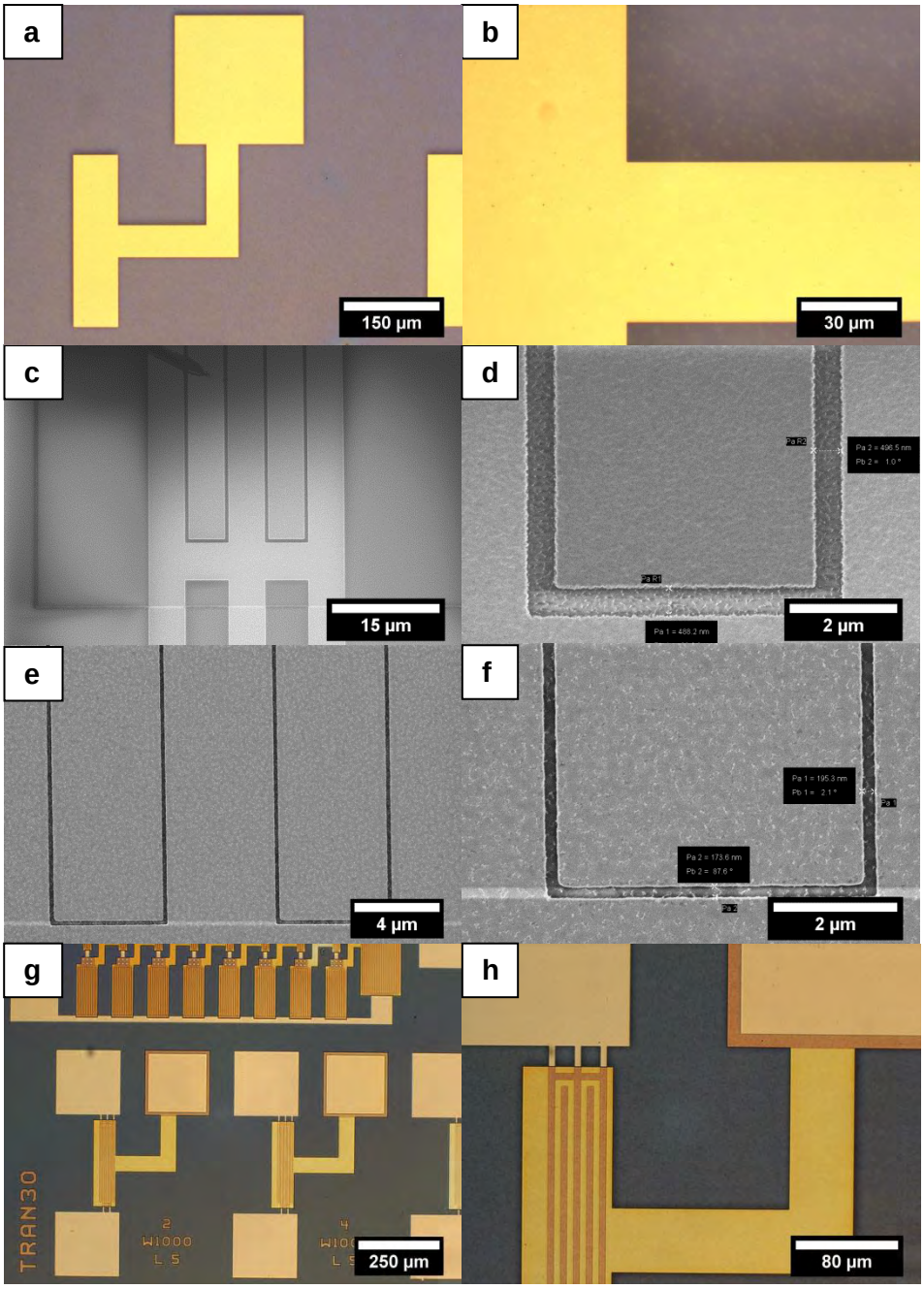



**Figure 5.3** (a-b, g-h) Optical microscopy and (c-f) SEM images of the different stages of the fully UV NIL-patterned TFTs on PEN foil. (a-b) First imprinted layer: 70 µm wide gate. (c-f) Second imprinted layer: 5 µm source-drain fingers with a line spacing of (c, d) 500 nm and (e, f) 200 nm. (g-h) Third imprinted layer: 180 x 180 µm² contact holes through the dielectric to the gate. Also shown are the 5 µm wide and spaced source-drain fingers.

The gate dielectric was, as in many electronic devices, a critical parameter strongly influencing the quality of the TFTs. As dielectrics for the flexible TFTs, oxides ($Al_2O_3$ and $SiO_2$) and organic materials (SU8, Parylene C) have been tested. SU8 is readily available in the semiconductor industry, has a high chemical resistivity, thermal stability and dielectric strength.[34] However, in our case, SU8 was disqualified as dielectric due to the thermal expansion mismatch to the FOC, resulting in a too strongly bowed FOC after SU8 spincoating and soft bake at 95°C. Parylene C on the other hand, could be deposited in a 150 nm thick layer by vapor deposition polymerization at a substrate temperature near room temperature. Parylene C has a high dielectric strength, high chemical and moisture resistance, and provides a hydrophobic surface beneficial for pentacene growth.[34] Unfortunately, as Parylene C is an organic material, it appeared sensitive to the here performed etching steps. Resist strip-off after source-drain and contact hole patterning simultaneously removed the dielectric due to a nearly identical etch rate of 100 nm/min of resist and Parylene C. Regarding the two tested electron beam-evaporated oxides, $SiO_2$ appeared superior over $Al_2O_3$. Therefore, $SiO_2$ was used as the dielectric in all devices described below.

As the TFTs were made in a bottom-contact, bottom-gate architecture, the final layer added to the device was the organic semiconductor. A pentafluorobenzenethiol (PFBT) SAM was deposited on all gold contacts to improve the charge injection.[35] Trichlorophenylsilane (TCPS) was deposited on all oxide surfaces to reduce electron trapping at the oxide interface. SAMs are known to improve the molecular order of the deposited semiconductor.[36] A blend of TIPS pentacene:PS in a 2:1 w/w ratio was inkjet-printed onto the interdigitated source-drain fingers, leading to TIPS pentacene crystals grown from the edge to the center of the inkjet-printed droplets (Figure 5.4).[30]

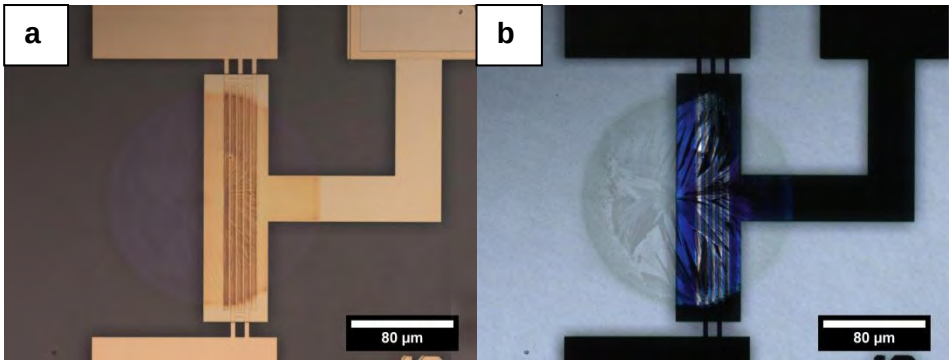



**Figure 5.4** Optical microscopy images (a, regular; b, with cross-polarizers) of flexible bottom-contact, bottom-gate TFTs with the entire metal-insulator-metal (MIM) stack patterned by SFIL and inkjet-printed TIPS pentacene/PS crystals after SAM deposition of PFBT and TCPS, on the interdigitated 5 µm wide and 2.5 µm spaced source-drain fingers, showing a crystal growth from the edge to the center of the droplet.

### 5.2.3 Electrical Characterization

To demonstrate the feasibility of the here developed multilayer imprinting process, SFIL-patterned TFTs on Si and PEN foil were electrically characterized in a non-illuminated glove box under $N_2$ atmosphere. The gate voltage was varied from 10 V to -10 V in a double scan and the bias over source and drain ($V_{DS}$) was held at -10 V. Transfer and output characteristics of fully UV NIL-patterned TFTs with a channel width of 1000 µm and length of 5 µm arranged in a comb structure, and the corresponding square route of $I_{DS}$, were recorded. First, results for the TFTs on Si will be shown and discussed (Figure 5.5a-b).

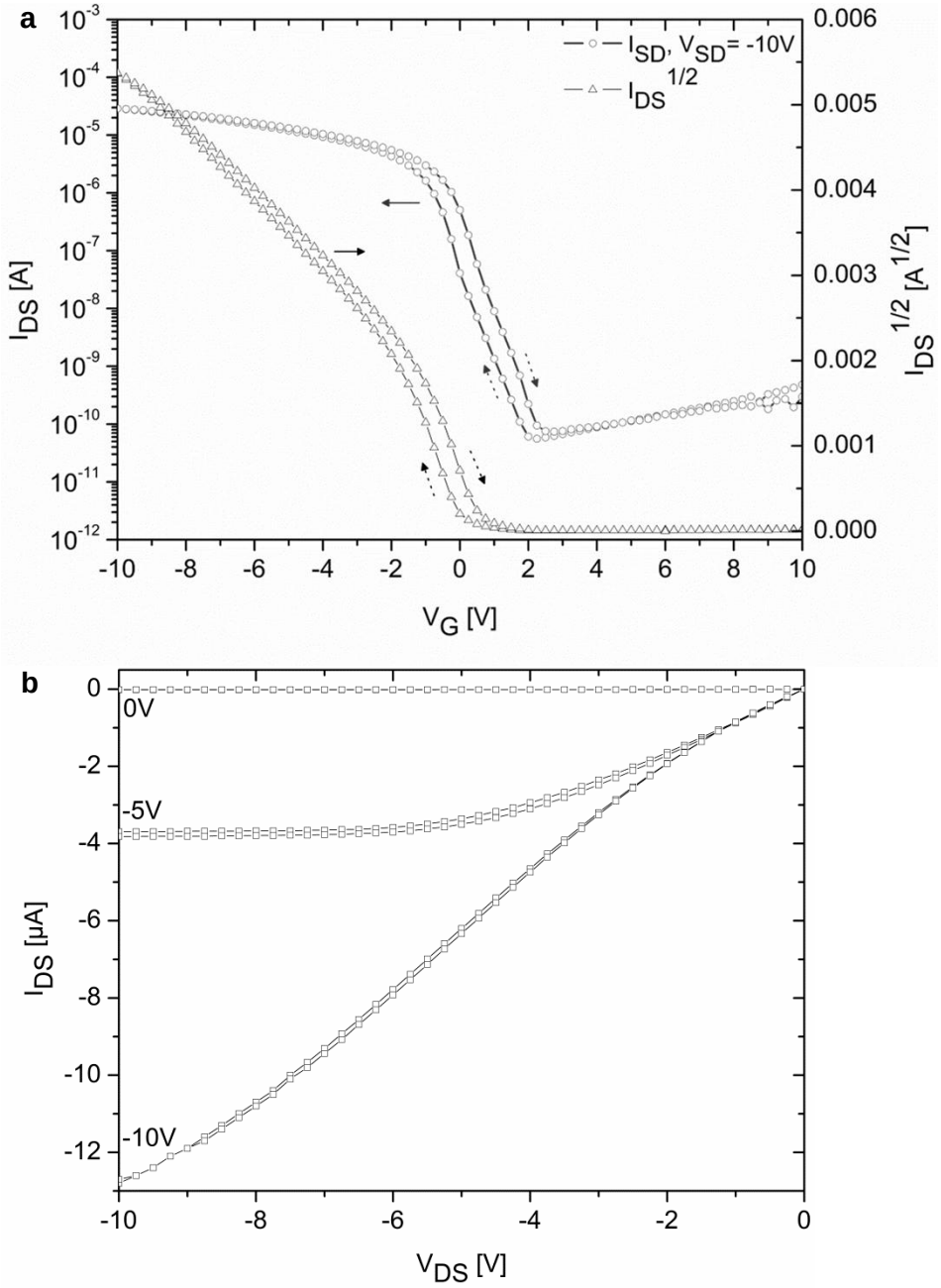



**Figure 5.5** (a) Transfer characteristics and the corresponding plot of the square root of $I_{DS}$ of one fully UV NIL-patterned bottom-contact, bottom-gate TFT on Si. Channel length and width are 5 and 1000 µm respectively. A 150 nm thick $SiO_2$ layer served as the gate dielectric, and a blend of TIPS pentacene/PS as the semiconductor. (b) The output characteristics of a TFT on Si with a gate voltage between 0 and -10 V at a step of 5 V.

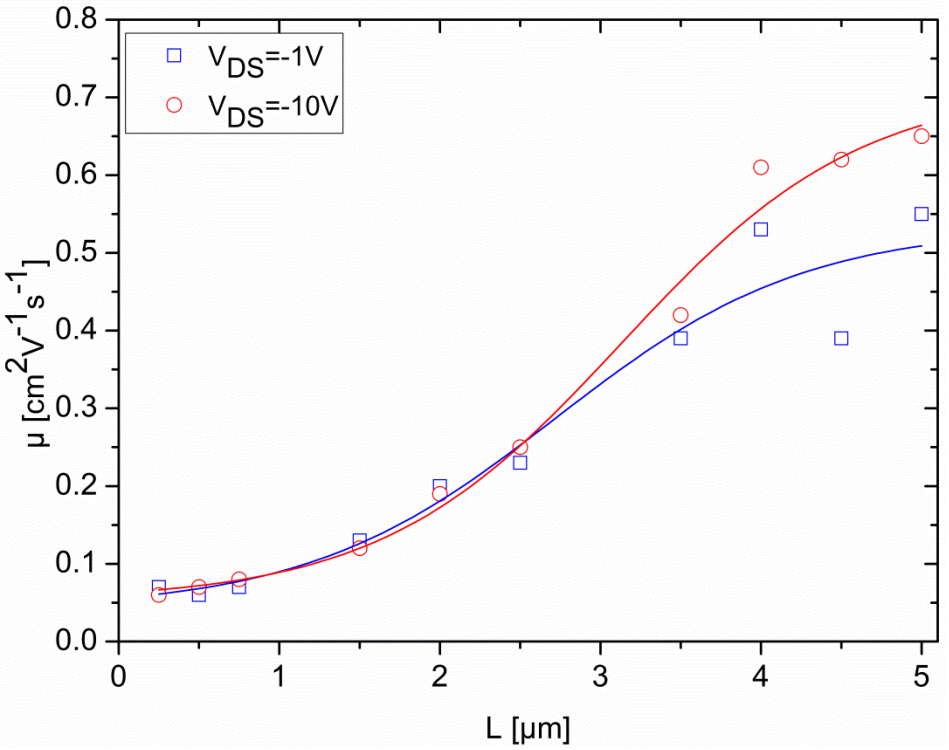



**Figure 5.6** Mobility μ at $V_{DS}$= -1 V (blue) and -10 V (red) as a function of the channel length L for the fully UV NIL-patterned TFTs on Si. The trend of the mobility is indicated by the s-shaped curves.

From the semi-logarithmic plot ($I_{DS}$ vs. $V_G$; Figure 5.5a), an on/off ratio of $5x10^5$, a sub-threshold swing of 0.7 V/dec and a low switch-on voltage of $V_{SO}$= 1.3 V for the TFT on Si have been calculated. The switch-on voltage was taken as the gate voltage at which the drain current is one order of magnitude higher than the off-current $I_{off}$.[28] From the plot of the square root of $I_{DS}$ vs. $V_G$ (Figure 5.5a), a high gate-dependent mobility of $\mu_{sat}$= 0.65 ± 0.16 $cm^2V^{-1}s^{-1}$ (average over four TFTs) and a maximum of $\mu_{SAT}$= 0.92 $cm^2V^{-1}s^{-1}$ at $V_G$= -0.75 V have been determined. The field-effect mobility was thereby calculated from Equation 5.1, with $V_{DS}$= -10 V:

$$\mu_{SAT}(V_G) = \frac{2L}{W \cdot C_i}\left(\frac{\partial\sqrt{I_{SD}(V_G)}}{\partial V_G}\right)^2 \qquad (5.1)$$

where $C_i$ is the capacitance per unit area of the gate dielectric layer, and L and W are channel length and width, respectively. The electrical

characteristics of the here fabricated fully UV NIL-patterned, bottom-contact, bottom-gate TFTs on Si are in good agreement, and in many cases improved in comparison to reported values in literature. Common gate TFTs with the same TIPS pentacene/PS blend (67wt%) inkjet-printed on photolithography patterned, golden source-drain electrodes on highly doped $n^{++}$ Si wafers with a 140 nm thermally grown $SiO_2$ gate dielectric, showed a slightly higher mobility of $\mu_{SAT}$= 0.72 ± 0.17 $cm^2V^{-1}s^{-1}$ (average over 73 TFTs) for a channel length of 5 μm.[30]

The here developed UV NIL-based patterning strategy allowed downscaling of the channel length into the low sub-micron regime. TFTs with a channel length as small as 250 nm have been fabricated. To our knowledge, this is the first report of such a small channel length with the here utilized, inkjet-printed blend of semiconductor TIPS pentacene and PS. Further downscaling is limited by the e-beam written patterns in the template, not by the imprint process itself. The plot of the mobility at $V_{DS}$= -1 V and -10 V as a function of the channel length L (with 250 nm < L < 5 μm) (Figure 5.6), shows a decrease in the mobility with decreasing channel length. The observed trend indicates the existence of a contact resistance, turning more dominant for smaller channel lengths. The non-linear slope in the corresponding $I_{DS}/V_{DS}$ plot (Figure 5.5b) confirms this contact resistance. A thin PS layer deposited directly on top of the Au contacts by phase separation from the semiconductor blend upon inkjet printing might be the origin of the experienced contact resistance.[31] Very recently,[37] it has been reported that PS accumulates at the center of the droplet upon evaporation of the TIPS pentacene/PS blend, resulting in less semiconductor in the center of the droplet. As the droplet size is the same for all TFTs, the insulating PS plays a more dominant role in the performance of the TFTs with decreasing channel lengths.

Next, we used the here engineered process, with imprint planarization (Scheme 5.2) to demonstrate flexible TFTs on PEN foil. The transfer, output characteristics and the corresponding square root of $I_{DS}$, are shown in

Figure 5.7a-b. The mobilities as function of the channel length from 5 µm down to 500 nm are given in Figure 5.8.

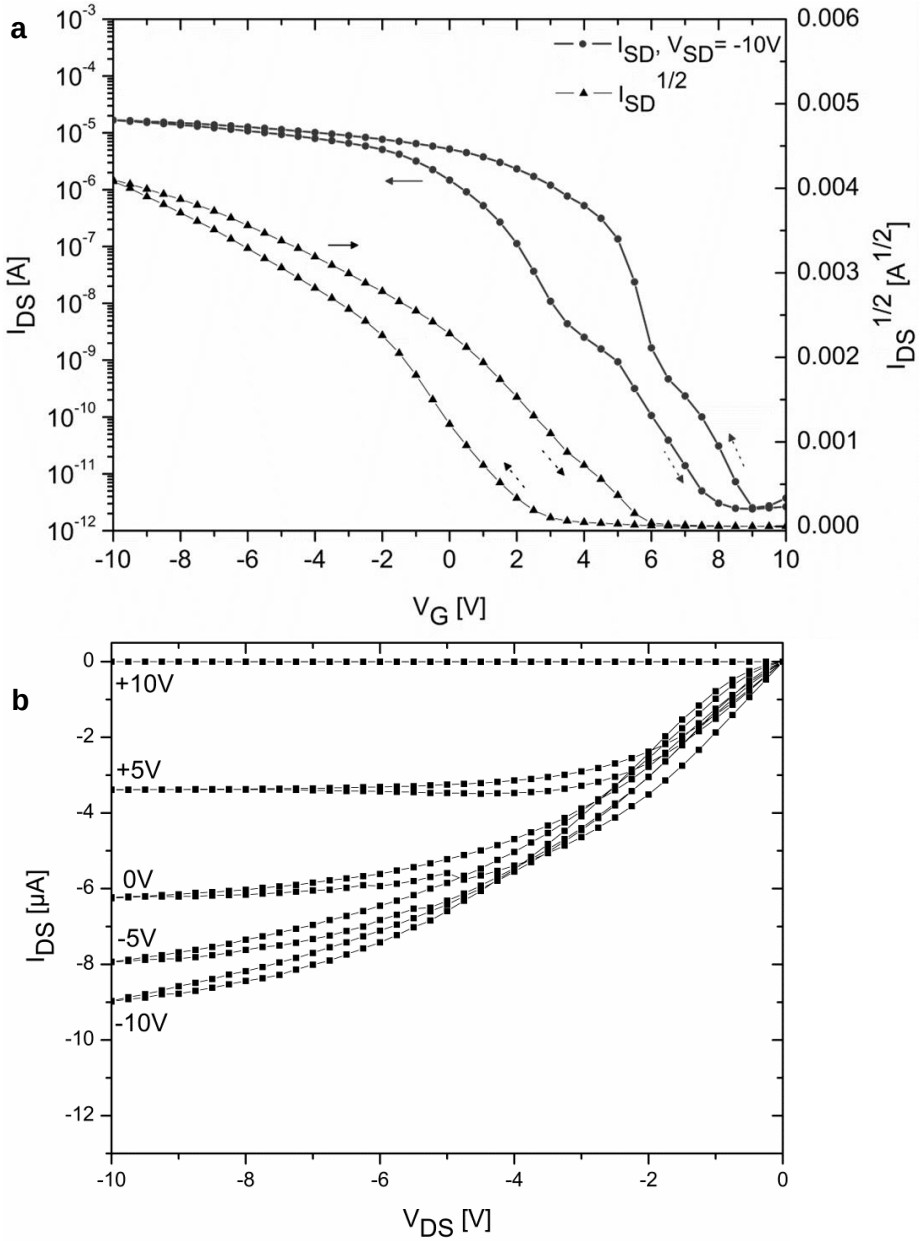



**Figure 5.7** (a) Transfer characteristics and the corresponding plot of the square root of $I_{DS}$ of one fully UV NIL patterned bottom-contact, bottom-gate TFT on PEN. Channel length and width are 5 and 1000 µm respectively. A 150 nm thick $SiO_2$ layer served as the gate dielectric, and a blend of TIPS pentacene/PS as the semiconductor. (b) The output characteristics of a TFT on PEN with a gate voltage between +10 V and -10 V at a step of 5 V.

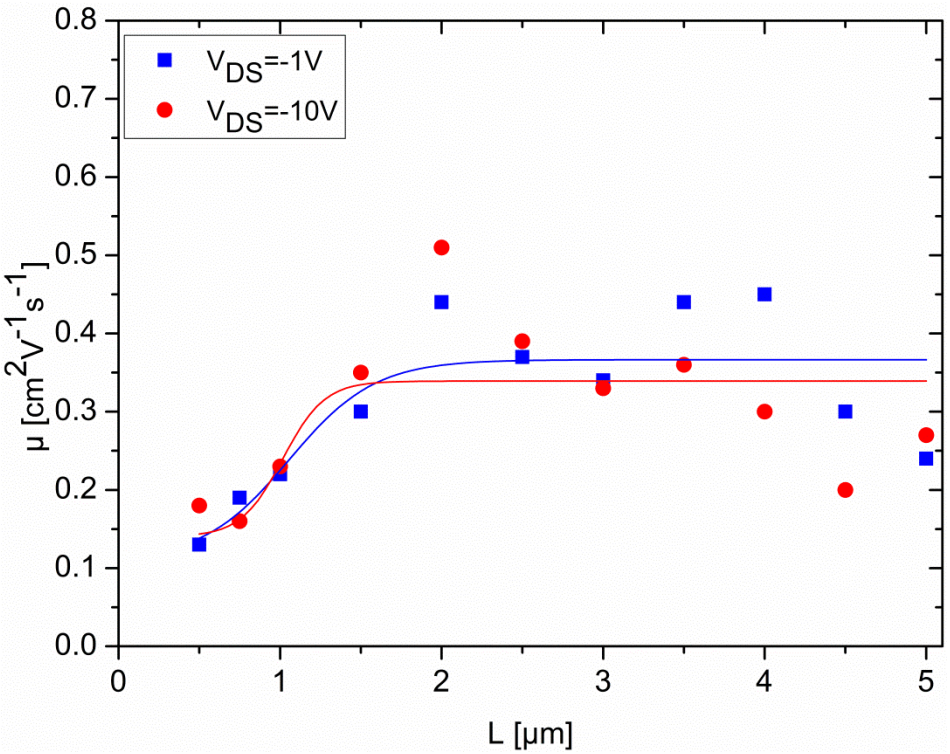



**Figure 5.8** Mobility at $V_{DS}$= -1 V (blue) and -10 V (red) as a function of the channel length L for the fully UV NIL-patterned TFTs on PEN foil. The trend of the mobility is indicated by the s-shaped curves.

From the semi-logarithmic plot ($I_{DS}$ vs. $V_G$), an on/off ratio of $7x10^6$, a sub-threshold swing of 0.9 V/dec and a switch-on voltage of $V_{SO}$= 7.4 ±0.7 V for the flexible TFTs have been calculated. From the plot of the square root of $I_{DS}$ (Figure 5.7a), a gate-dependent mobility of $\mu_{sat}$= 0.20 $cm^2V^{-1}s^{-1}$ at $V_G$= -0.50 V (average over four TFTs: $\mu_{SAT}$= 0.27 ± 0.05 $cm^2V^{-1}s^{-1}$) has been determined. The on-current at $V_G$= -10 V is comparable to the data obtained for the TFT on Si (Figure 5.5a), but significant differences are visible in the switch-on voltage, hysteresis and mobility. The TFTs on Si and PEN foil have an identical device architecture and are fabricated with the same process, except for the additional imprinting of the planarization layer and oxide etch stop deposition in case of the flexible TFTs. The positive shift of the switch-on (and off) voltage and the observed hysteresis in the transfer characteristics of the flexible TFT (Figure 5.7a), are a result of charge trapping at the oxide – semiconductor interface.[39-40] Actually, a slightly

different spreading of the semiconductor during inkjet printing was observed, which indicates a differently packed silane (TCPS) layer on the dielectric ($SiO_2$) for both substrates. The droplet spread more on the TFTs on Si, although the inkjet printing was identical. Therefore, the area of the semiconductor not controlled by the gate is larger for the TFTs on Si, interfering more with the device performance. Current can flow in an uncontrolled fashion from the source to the semiconductor, having a negative effect on the off-current. On the foil, spreading was less, leading to fewer leakage paths and thus a superior low off-current (Figure 5.7a). Reduced spreading of the same ink volume results thus in a thicker TIPS Pentacene/PS layer on the foil. Therefore, the shoulder-like behavior seen in the I/V curve for the flexible TFTs might be explained by a backchannel effect.

The electrical characteristics of the here fabricated TFTs are comparable to earlier reported values in literature with photolithographically patterned bottom-contact, bottom-gate TFTs on PET foil and a sputtered $Al_2O_3$ gate dielectric with an average saturation mobility of $\mu = 0.22 \pm 0.05$ $cm^2V^{-1}s^{-1}$.[38] Flexible TFTs with a small channel length down to 500 nm have also been fabricated on foil. Plotting the mobility at $V_{DS} = -1$ V and -10 V vs. the channel length shows a transition point at $L = 1.5$ µm (Figure 5.8). The drop in the mobility below $L < 1.5$ µm indicates a limited charge injection, which is supported by the non-linear plot of the square root of $I_{DS}$ vs. $V_G$ (Figure 5.7a). Furthermore, charge injection is limited due to the ink blend properties, as discussed for Si previously.

The results shown here confirm that high-quality bottom-contact, bottom-gate TFTs have been made by patterning the entire metal-insulator-metal (MIM) stack with UV NIL on PEN foil with channel lengths as small as 500 nm on foil, holding promise for facile R2R production.

## 5.3 Conclusions

In this chapter, the feasibility of UV NIL as a patterning technique for the fabrication of multilayered, electronic devices on Si and PEN foil has been shown. Bottom-contact, bottom-gate TFTs have been fabricated as demonstrators by patterning the entire MIM stack of the TFT by UV NIL, forming the gate, source-drain and contact hole with an alignment precision of 25-200 nm on Si and 50-300 nm on foil. We could only successfully and reproducibly pattern all three layers of the TFT on foil by introduction of imprint planarization, allowing a controlled and homogeneous residual layer thickness. A further conclusion of this work is, that the dielectric should match the coefficients of thermal expansion of the foil-on-carrier system (excluding SU8) and should withstand or at least show a high etch selectivity to the imprint resist upon reactive ion etching and resist strip-off (excluding Parylene C). The performance of the TFTs on Si and PEN foil with the largest channel length (L= 5 μm) is comparable with state-of-the-art devices fabricated by photolithographic patterning.[30, 38] By downscaling the channel length, TFTs with a minimal channel length of 250 nm on Si and 500 nm on PEN foil have been demonstrated.

The final flexible TFT fabrication process is envisioned to be R2R imprinting. The critical overlay of the source-drain and gate cannot be accurately enough controlled in a R2R process. Therefore, efforts are undertaken to develop a self-aligned imprinting process, implementing the fabrication lessons learned here with the room temperature, low pressure and high precision technique SFIL.

## 5.4 Experimental Section

### 5.4.1 Materials and Methods

Imprint resist MonoMat and anti-sticking layer RELMAT™ were purchased from Molecular Imprints, Inc. An experimental poly(ethylenenaphthalate)

foil (PEN, 25 µm thick) was provided by Holst Centre. 6,13-Bis(triisopropyl-silylethynyl) pentacene (TIPS pentacene) was synthesized according to literature.[41] Polystyrene (PS) (Mw≈ 9.58 kDa, PDI= 1.03) was purchased from Fluka. 1,2,3,4-Tetrahydro-naphthalene (tetraline) was purchased from Merck.

### 5.4.2 Foil-on-Carrier (FOC)

FOCs have been made by reversibly laminating the PEN foil with a glue to a double-side polished Si wafer at a temperature <95°C. The foil was cut according to the size of the carrier (4 in Si wafer) and thermally cured by heating for 1 h at 170°C in a convection oven.

### 5.4.3 Step-and-Flash Imprint Lithography (SFIL)

The UV-transparent quartz templates used for the experiments were fabricated by standard e-beam lithography and RIE techniques. The templates contained, on an active area of 11 x 11 $mm^2$, test features in the dimensional range of 100 nm up to 750 µm and the TFT features with channel lengths from 5 µm down to 250 nm with a depth of 300 nm.

SFIL was performed with an Imprio 55 tool from Molecular Imprints, Inc. The imprints were carried out at room temperature and under a force of 3 N. For improved adhesion of the drop-dispensed imprint resist (MonoMat™), a BARC layer of DUV30J was spincoated on the surfaces at 3000 rpm for 1 min and baked for 2 min at 120°C. MonoMat™, after field by field drop-dispensing on the substrate, filled the template within 60 s and was cured through the backside of the template for 3 s with broadband UV light (exposure dose of 80 $mJ/cm^2$ and $\lambda$= 230-360 nm).

### 5.4.4 Dry Etching

Anisotropic $O_2$ plasma-based reactive ion etching was performed in a home-built tool (Tetske) at a chamber pressure of 10 mTorr and 20 sccm $O_2$ at 20 W to remove the thin residual layer within 1 min and to strip-off

the resist after processing within 2 min. Unprotected metal (Cr and Au) and dielectric of the MIM stack were removed by Ar ion beam etching with an Oxford Ionfab 300, removing the metal layer within 5 min and the 150 nm $SiO_2$ within 10 min, controlled by an endpoint detection system.

## 5.4.5 Dielectric Deposition

Parylene C was deposited with a dedicated Parylene coater (SCS Labcoter 2 Parylene Deposition System 2010). SU8-5 (MicroChem) has been deposited by spincoating for 10 s at 500 rpm and 30 s at 4000 rpm followed by a soft bake program starting at 25°C, holding the temperature 1 min at 50°C, 1 min at 65°C and 3 min at 95°C after which the temperature was slowly decreased to 25°C. An SU8 layer thickness of 4.1 µm has been obtained. $SiO_2$ and $Al_2O_3$ were evaporated in a Balzers evaporator (BAK600) using an 8 kV e-gun beam at a pressure of $9x10^{-7}$ bar resulting in a deposition rate of 3-5 Å/s.

## 5.4.5 Self-Assembled Monolayers

PFBT was deposited by 15 min dipping of the sample into a PFBT (10 mM) solution in ethanol, followed by rinsing with ethanol and $N_2$ blow drying. $N_2$ was utilized as carrier gas bubbling through TCPS in a closed chamber at atmospheric pressure for 15 min to deposit TCPS from the gas phase on all oxide areas. The substrates were baked 2 min at 100°C on a hot plate after flushing the chamber with $N_2$ to remove the side product (hydrochloric acid) of the condensation reaction.

## 5.4.7 Semiconductor Deposition

An inkjet printing setup with a high-precision vertical translation stage and a Microfab glass nozzle (type MJ-ATP-01-50-DLC, 50 µm orifice diameter) was used to print the blend of TIPS pentacene (20 mg/ml) :PS (10 mg/ml) in a blending ratio of 2:1. Droplets with a volume of 50 pL were jetted on demand, onto transistor substrates kept at a temperature of 70°C. All printing experiments were performed in ambient cleanroom conditions.[30]

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## Chapter 6

# Selective Material Deposition in Open Microchannels

*A novel method to selectively deposit functional materials from solution into open microchannels is reported in this chapter. Microchannels were made by embossing in SU8 deposited on poly(ethylene terephthalate) foil. The deposition mechanism was studied by using the dye rhodamine 6G as a solute. Capillary assembly is proposed as the dominant filling mechanism, based on the observed results which show a feature size-dependent filling. As a functional solute, a Pd salt has been deposited in the open microchannels. The Pd salt was reduced in a subsequent step to Pd particles, catalyzing the electroless deposition of Cu forming conductive microwires. The here developed method opens the route to faster and cheaper plastic electronics.*

Part of this work has been published in D. Turkenburg, H. Rendering, A. Hovestad, N. Stroeks, P. Maury, P. F. Moonen, J. Huskens, I. Barbu, E. R. Meinders, *Mater. Res. Soc. Symp. Proc.* **2011**, *1288*, mrsf10-1288-g09-05.

## 6.1 Introduction

Flexible electronics offer cost and functional advantages, like conformability, flexibility, rollability and even stretchability. These will push the limits of material performance, process and system integration, and circuit design to demonstrate the full potential of flexible electronics.[1] Thin film transistors (TFTs) are a key component for flexible electronic applications[1] such as flexible displays. Typically, these functional devices are made of patterned stacks of metals, semiconductors and insulators. In particular if plastic substrates are used, the dimensional instability of the plastic substrate needs to be controlled to allow high-resolution patterning. However, high-resolution alignment of the micro- and nanopatterns relative to each other remains a major challenge, especially on flexible foils, as the functional layers of the electronic device are layer-by-layer deposited and processed.

When the critical components are self-aligned, high-resolution alignment steps become obsolete and production costs are reduced. Several technologies have been reported in this direction. In self-aligned imprint lithography (SAIL),[2] the blueprint of a TFT is patterned by imprint lithography. Alignment is designed into the template and transferred by the imprinting step into the substrate on which the TFT is patterned. HP has developed[2] a top-down method where a stack of resist masks is deposited on an unpatterned stack of materials. A multi-level template is used to structure a resist layer deposited on top of this stack of materials. One by one, each level of the mask is used to pattern one of the underlying materials, making it a purely subtractive process. Dickey *et al.*[3] have described an elegant but rather complex process making use of the angle-dependent shadows of a tilting resist mask to achieve self-alignment. Using the gate pattern of a transistor as a mask for the development of the source-drain level is another, rather specific, case of self-alignment.[4] Self-aligned gate architectures, defined by exposure of a photoresist using two

densely packed inkjet-printed gold electrodes have been reported as well.[5]

Next to the above described top-down patterning techniques, self-alignment can be achieved by capillary forces in a bottom-up approach to control the self-assembly of materials, yielding an additive patterning technique. In micromolding in capillaries (MIMIC), first reported by Whitesides *et al.* in 1995,[6] capillaries are formed by placing a soft elastomeric stamp, usually made of PDMS, with parallel protrusions on a smooth surface. The grooves form channels (capillaries), which are spontaneously filled with a solution as an effect of capillary pressure upon placement of a drop of the solution at the open end of the capillary. After complete solvent evaporation, the stamp is removed leaving the patterns on the substrate. Upon gradual solvent evaporation in the channels, a meniscus is formed under the roof of the stamp channels by the capillary forces. Depending on the solute concentration, two kinds of patterns can be obtained. In the high concentration regime, the solution reaches supersaturation when the channel is still filled with solution resulting in deposition of solute on the entire bottom of the channel. In the dilute concentration regime, supersaturation is reached when most of the solvent has evaporated, and the volume of the residual solvent is not enough to fill the channel completely. In this case, the meniscus forms a U-[7] or W-shape[8] in the channel, dragging under capillary force the solute to the edges of the channel, where it accumulates and aggregates forming defects in the stripes or creating split lines.[9] Due to the mechanical instability of the soft polymeric stamp, the dimensions of the channels in MIMIC are typically limited to about a few hundred nanometers.[10] Large area, sub-100 nm patterns have been made by nanomolding in capillaries (NAMIC),[10-11] in which a hybrid stamp with harder, well-defined features fabricated by nanoimprint lithography (NIL)[12-13] on flat PDMS has been applied.

The physical assembly of particles from a suspension onto patterned and non-patterned substrates has been described by convective[14] or capillary

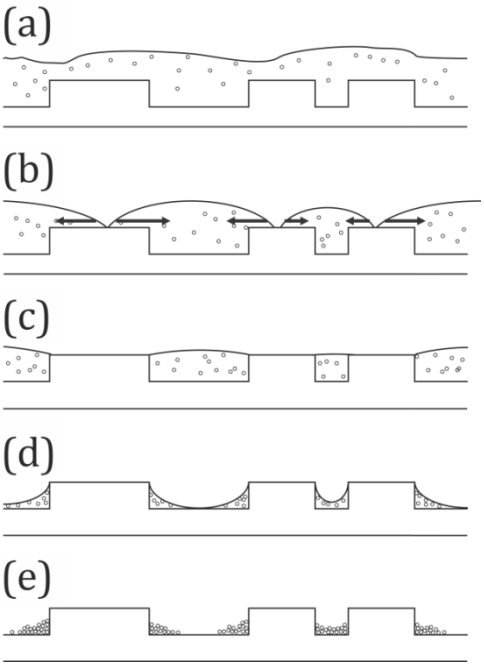
assembly.[15] In the latter case, small particles are assembled from suspension by forces in a moving meniscus that drive them into shallow recesses.[16] In convective flow, the assembly process is driven by hydrodynamic forces induced by an influx of water upon water evaporation, close to the meniscus three-phase contact line. The assembly process starts when the thickness of the solvent layer becomes equal to the particle diameter.[14] Convective flow can be observed by contact angles up to 20°.[17] On more hydrophobic surfaces, with a contact angle between 20 and 60°, capillary assembly is observed.[17] The component of the force exerted by the meniscus parallel to the substrate increases and becomes sufficiently strong to prevent particle deposition on flat surfaces. The parallel force of the contact line being dragged over the substrate can be counteracted by a vertical capillary force arising on patterned surfaces, pinning and deforming the liquid meniscus around the structures. Geometrical trapping at the substrate features and capillary forces exerted during film breakage lead to one or a small number of particles being confined close to the obstacle.[17] As a result, particles are trapped at the step edges of the template features, whereas no deposition occurs in the surrounding areas.

Here reported are initial results obtained for the selective deposition of solutes in open microchannels embossed in SU8 deposited on a poly(ethylene terephthalate) (PET) foil by nanoimprint lithography (NIL). Rhodamine 6G has been deployed as the solute, showing line splitting upon evaporation in the open microchannels, which is typical for MIMIC in the low concentration regime. As a functional material, a Pd salt has been selectively deposited on large area on a patterned, non-functionalized PET foil. In a subsequent step, the Pd salt has been reduced to form Pd particles, which catalyze the electroless deposition of copper, forming conductive metal microwires.

## 6.2 Results and Discussion

### 6.2.1 Process Scheme

We here report the selective deposition of molecules and particles in embossed microchannels. The process can be divided in several steps (Scheme 6.1). In the first step (Scheme 6.1a), a suspension of particles is deposited on the patterned surface. Upon evaporation of the solvent, the fluid film breaks and a three-phase contact line is formed between the substrate, suspension and air (Scheme 6.1b). Upon further evaporation, particles are dragged into the channels by the moving contact line, and pinned to the edges of the embossed channel (Scheme 6.1c). Depending on the feature dimensions, the vapor pressure of the solvent and the particle size, the particles are dragged into the edges of the channel by capillary force induced by the U-shaped meniscus at nearly completed solvent evaporation (Scheme 6.1d). After complete solvent evaporation, the particles are deposited at the edges of the feature or spread over the entire channel (Scheme 6.1e).




**Scheme 6.1** Illustration displaying the proposed selective deposition process of particles in open micro-channels. (a) Solution deposition is followed by (b) breaking of the fluid film and formation of a three-phase contact line, confining (c) the particles into the channels. Upon solvent evaporation (d), a U-shaped meniscus is formed, dragging the particles by capillary forces into the edges of the channel. (e) Narrow channels are evenly filled, while wide channels show particles concentrated at the edges.

Several parameters influence the selective deposition, such as the surface energy and structural parameters (width, depth and curvature of the edge) of the substrate, the fluid parameters (boiling point, vapor pressure and viscosity) and the solute parameters (particle size, adhesion properties, solubility in solvent). Moreover, the solvent should not dissolve or permeate through the substrate material and none of the materials should be extremely costly or toxic to allow easy large scale application. Finally, also the deposition method (pretreatment, drop casting, spin coating, dip coating, temperature, humidity, etc.) may influence the process.

With these prerequisites in mind, SU8 was chosen as the base material in which the structures were replicated. SU8 is readily available in the semiconductor industry, has a high chemical resistivity and thermal stability. To investigate the effect of geometry, a pattern of lines and squares with features of 1-20 µm width and space was transferred into the SU8 base material by hot embossing. The depth of the embossed trenches (Figure 6.1a) was determined by profilometry to be 700 nm (Figure 6.1b), whereas the total thickness of the SU8 layer was 5 µm after spincoating. The open microchannels reach therefore not to the substrate surface and expose only SU8 interfaces. Silicon wafers as well as PET foil reversibly laminated to a Si wafer (foil-on-carrier, FOC) have been used as substrates.

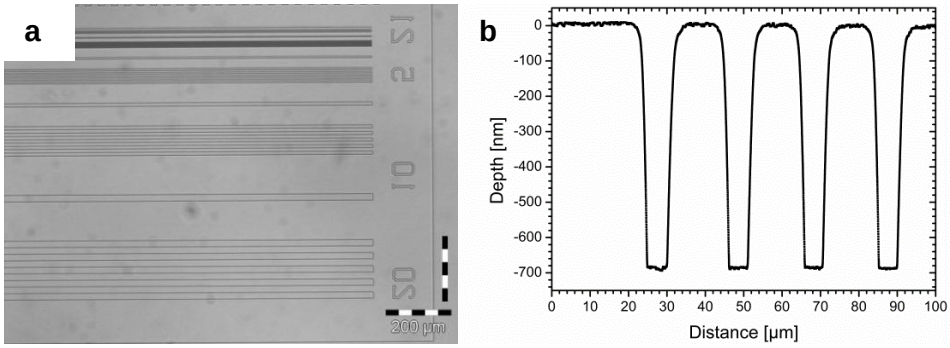



**Figure 6.1** (a) Optical microscopy image showing trenches with 1, 2, 5, 10 and 20 µm width embossed in SU8 deposited by spincoating on Si wafer. (b) Graph showing the depth of the embossed 5 µm wide trenches in SU8 recorded by profilometry.

Several fluids have been studied for their wetting, filling and evaporation behavior. Fluids with intermediate surface tension (Table 6.1) were found to be favored. The surface tension of ethanol was too low, resulting in completely wetted substrates showing no specific film breakage and evaporation process. No selective particle deposition could be obtained, because the meniscus could not be pinned to the pattern edge to drag the particles into the cavity. With increasing surface tension the tendency of the liquid film to break up became stronger. At too high surface tensions however, as was the case with water, the fluid tended to adopt a spherical shape (droplet) and did not conform to the underlying microstructure anymore. Mixing two (or more) solvents allowed tuning of the surface energy. However, due to different evaporation speeds, the overall surface energy of the solvent mixture was changed during the drying and deposition process.

**Table 6.1** Solvent properties, data from CRC Handbook of Chemistry and Physics.[18]

| | **Surface tension at 25°C [mN/m]** | **Vapor pressure at 25°C [kPa]** |
|---|---|---|
| **Ethanol** | 21.97 | 7.87 |
| **n-Butanol** | 24.93 | 0.86 |
| **Acetic acid** | 27.10 | 2.07 |
| **2-Methoxy ethanol** | 30.84 | 1.31 |
| **Water** | 71.99 | 3.17 |

The speed of the retracting contact line of the fluid front, dragging along the solute, plays an important role in determining the deposition selectivity. Upon (too) fast evaporation, an uneven settlement of the solute was observed. As the evaporation speed depends on the vapor pressure, many commonly used solvents with the proper surface tension have to be excluded. Figure 6.2 displays a selectively retreating fluid front of butanol (without solutes) on embossed SU8 patterns on a Si wafer. Butanol forms a contact angle of <10° with unpatterned SU8 and bulk solvent evaporation is shortly followed by evaporation in the channels. As the capillary pressure

($p_c$) is linearly related to the cosine of the contact angle ($\theta$),[19] the surface tension ($\gamma$), and the inverse of the effective radius of the spherical meniscus ($r$) via the Young-Laplace equation in spherical form (Equation 6.1), the narrower microchannels having a smaller effective radius remain filled longer than the wider ones due to the larger capillary pressure experienced (Figure 6.2). Further study of the contact angle at the boundary of the features has not been conducted here.

$$p_c = \frac{2\gamma cos\theta}{r} \tag{6.1}$$

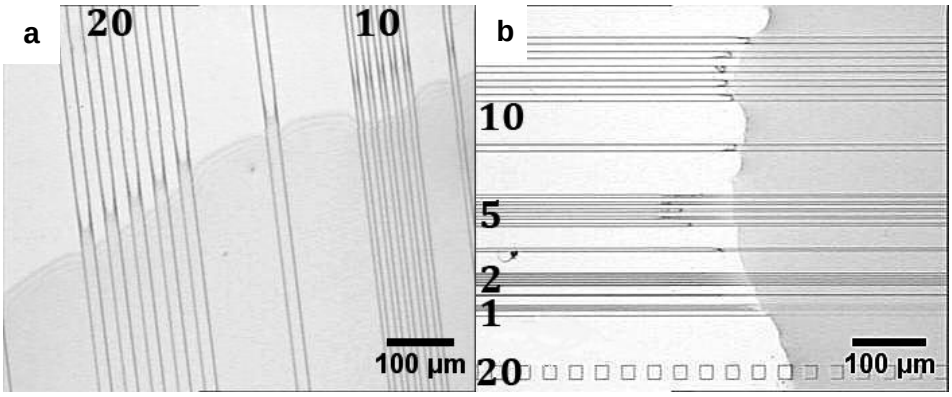



**Figure 6.2** Optical microscopy images of a retreating n-butanol front on an SU8 surface with imprinted microchannels in the indicated dimensional range of (a) 10 and 20 µm and (b) 1-20 µm.

## 6.2.2 Filling Mechanism in Open Microchannels

To study the filling mechanism occurring in the open microchannels, the dye rhodamine 6G was added as a solute to the solvent, as it is easily detected under a microscope at low concentrations because of its strong absorption in the visible range. The surface tension of the solvent is not significantly changed upon addition of low concentrations of the dye. Upon drying, rhodamine was selectively deposited in the structures as can be seen in Figure 6.3. The microscopy images show a geometry dependence. Smaller features, such as the narrow channels of 1 and 2 µm (Figure 6.3a),

are more evenly colored, indicating solute deposition over the entire channel width. In the larger features, represented by the wider trenches of 5 and 10 μm in Figure 6.3a and the 10 μm squares in Figure 6.3b, the solute is seen predominantly at the edges of the structure. From this observation, a capillary assembly deposition mechanism can be concluded, in which the solute deposits as a function of the contact angle formed by the meniscus in the channel. The contact angle in the narrower channels is dominated by the side walls, allowing uniform deposition in the channel. In the wider structures, the meniscus forms a U-[7] or W-shape[8] upon drying, prohibiting deposition in the center of the channel due to a too high contact angle. At the edges however, the contact angle is lower, allowing deposition of the solute under Stokes drag of the contact line. Another observation is the slight but significant deposition of rhodamine on the tops of the SU8 structures a couple of microns away from the channel feature edges. Physisorption of rhodamine, via the iminium sites,[20] just before final evaporation of the solution is believed to cause the observed deposition near the feature edges.

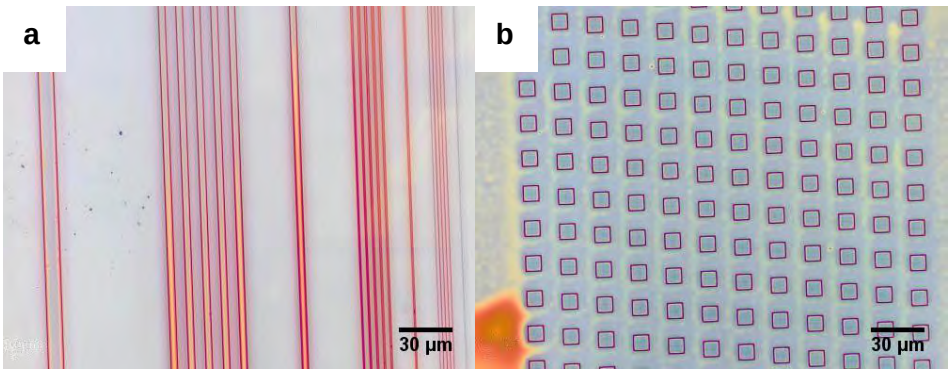



**Figure 6.3** Optical microscopy images of rhodamine 6G deposited into microchannels embossed in SU8 deposited on Si. (a) Narrow trenches of 1 and 2 μm are homogeneously filled, while the wider 5 and 10 μm trenches in (a) and the 10 μm wide squares in (b) show solute (rhodamine 6G) only at the edges of the structure.

### 6.2.3 Metal Wires by Functional Solute Deposition

Subsequently, a palladium precursor was employed as a functional solute instead of the fluorescent dye. A solution of a Pd salt in acetic acid was deposited on the patterned SU8 on PET by spincoating. After selective retraction of the solution into the microchannels and complete solvent evaporation, the Pd(II) salt was reduced to Pd(0) by submersion in a solution of 2.5 g/L borane dimethylamine complex in water for 10 min at 50°C. After gently rinsing with water and $N_2$ blow drying, Cu was selectively grown within 5 min from a conventional electroless deposition (ELD) bath. Pd particles served thereby as a catalyst for Cu growth.[21-22] Figure 6.4 displays Cu selectively deposited inside the embossed microchannels. With a growth rate of 80-100 nm/min, depending on the age of the bath, the narrower channels <2 μm connected already on some parts of the channel due to the small channel spacing (equal to the channel width) and overplating (Figure 6.4a). The single channels remained all isolated. Features >5 μm were completely filled with Cu and appeared not to be connected to each other. The Pd particles, selectively deposited at the edges of wider features according to the mechanism studied in the previous section, catalyze the Cu growth. As expected, the Cu growth was isotropic and continuous, allowing to close the gap in between the wide features by longer exposure to the ELD bath.

Over- and under-plating issues connecting multiple microwires or disconnecting single microwires, might be solved by optimization of the application process or the pattern itself. Options to be explored are deposition processes inducing a retracting contact line perpendicular to the channel width and increase of the channel spacing.

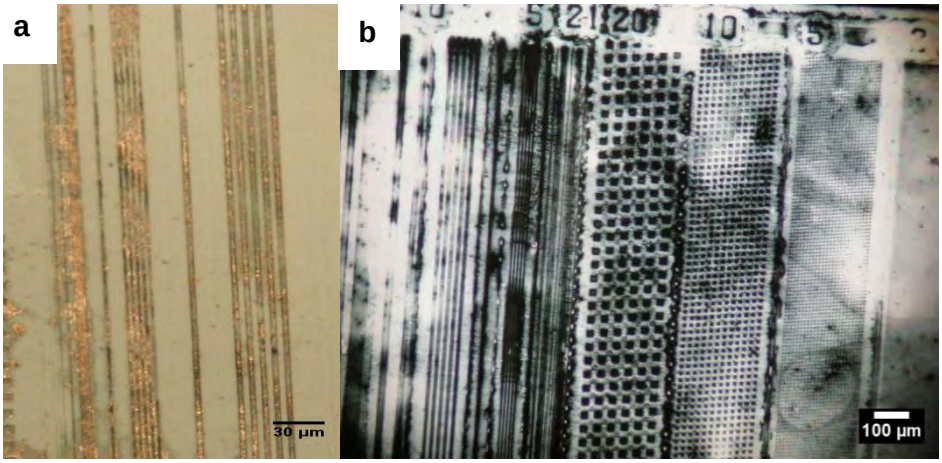



**Figure 6.4** Reflection (a) and transmission (b) optical microscopy images displaying the selective deposition of copper in embossed SU8 microcapillaries on PET foil having widths of (a) 1-5 µm and (b) 1-20 µm.

## 6.3 Conclusions

A novel method has been developed to selectively deposit materials from solution in open microchannels, patterned in SU8 by embossing. Rhodamine 6G in butanol has been applied to study the filling mechanism. A feature width dependence upon filling was observed. The solute was deposited over the entire pattern width for narrow (1-2 µm) features, while the solute was only deposited at the edges for wider (5-20 µm) features. Due to the observed channel width dependence upon filling, capillary assembly is proposed as the filling mechanism in which the width of the feature influences the contact angle and therefore the effective radius of the U-shaped meniscus in the channel according to the Young-Laplace equation. In a similar manner, Pd salts as precursor for Pd nanoparticles were deposited, serving as a catalyst for the electroless deposition of Cu, thus leading to metallic microwires.

This general approach can selectively steer active components of an electronic device by assembly into open microchannels, making expensive high-precision alignment and additional lithography processing (e.g. lift-off) obsolete. Furthermore, the here presented technique is roll-to-roll

compatible and therefore of great potential and interest for plastic electronics manufacturing.

## 6.4 Experimental Section

### 6.4.1 Materials

PET foil V109/2 100 µm (Agfa), 1H,1H,2H,2H-perfluorodecyltrichlorosilane (PFDTS, 97%, ABCR GmbH & Co.KG), SU8-5 (MicroChem), rhodamine 6G (95%, Aldrich), n-butanol (>98%, Fluka Chemie AG), 2-methoxyethanol (Shell), acetic acid (>99.7%, Sigma), palladium(II) acetylacetonate ($Pd(acac)_2$, 99%, Aldrich), borane dimethylamine complex (DMAB, 97%, Aldrich), and Enplate MID SELECT CU9070 (Enthone) have been purchased and used as received.

### 6.4.2 Template Manufacturing

Silicon templates have been made by optical lithography. Silicon wafers (4 in.) were spincoated with positive resist HPR504 and subsequently patterned using an ASML PAS 5500/100D stepper. After development of the exposed photoresist layer, the resist structures were transferred into silicon by reactive ion etching down to a depth of 700 nm. After resist strip-off in $O_2$ plasma, PFDTS was deposited on the templates by means of chemical vapor deposition to form an anti-sticking layer.

### 6.4.3 Thermal Imprint Lithography

As substrates, 4 in. silicon wafers and PET foil, reversibly glued to Si wafer carriers,[23] have been used. An SU8 layer of 5 µm was deposited on the substrates by spincoating 5 s at 500 rpm and 30 s at 3000 rpm, followed by a soft bake of 2 min at 95°C on a hotplate for solvent evaporation. Thermal imprinting was performed with the thermal imprinter *Eitre 6* from Obducat (Malmö, Sweden) at 95°C under 40 bar pressure for 240 s and crosslinking at 200°C under 20 bar pressure for 180 s. Template and substrate were

demolded at 80°C, leaving inverted patterns from the Si template in the SU8 layer. The residual layer was not removed.

### 6.4.4 Material Deposition

Dye deposition experiments were performed with a 0.1% (w/w) of rhodamine 6G in n-butanol, and a solution of 0.08-0.3% (w/w) of $Pd(acac)_2$ in acetic acid. Droplets of 20-40 µL were deposited on the structures and left to dry in air for selective deposition of a small area. For selective deposition on a larger area, samples were spincoated with the solution for 30-600 s at 400-2000 rpm. Samples with selectively deposited palladium were activated by submersion in a solution of 2.5 g/L DMAB in water during 10 min. at 50°C. Activated substrates were mildly rinsed with water before submersion for 1-5 minutes in an Cu electroless deposition bath made up of 200 ml/L MS CU 9070 (from *Enthone,* mixture of $CuSO_4 \cdot 5\ H_2O$ and NaOH) and 11 mL/L aqueous formaldehyde 48% at 40-48°C with air agitation.

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## Chapter 7

# Soft-Lithographic Patterning of Room Temperature-Sintering Ag Nanoparticles on Foil

*The scope of room temperature-sintering, poly(acrylic acid)-capped silver nanoparticles (Ag-PAA NPs) was studied in this chapter, regarding their use in a wide range of nanofabrication methods to form metallic silver structures on flexible poly(ethylene terephthalate) (PET) substrates. Silver wires were patterned on PET foil by MIMIC, and silver wires embedded in SU8 were fabricated on PET foil by wetting-controlled deposition in open microchannels. One hundred µm-wide Ag microwires with a length of 5 – 15 mm, height of 0.6 – 2.5 µm, and a maximum conductivity of a factor 7.3 lower than bulk Ag were obtained. The sintering depth was found to be limited to around 100 nm for HCl-vapor induced sintering. MeOH was studied as an alternative dispersing solvent. It sped up MIMIC drastically, but the low particle packing quality and pre-coalescence in solution resulted in a higher resistivity. NaCl, added in a concentration below 50 mM to the Ag-PAA NP ink, was investigated as alternative sintering agent, inducing self-sintering upon slow water evaporation. The feasibility of the Ag-PAA NP ink for repetitive printing of 3 µm-wide Ag dots with a hydrogel reservoir stamping system was studied as an alternative printing technique. Arrays of 144 Ag dots each were printed up to eight times on a PDMS substrate, with up to 17 defects in the last print, presumably as a result of clogging in the 5 µm-wide pores of the chip.*

## 7.1 Introduction

The fabrication of metallic, conductive structures in plastic electronics is an emerging field of research. A market with annual revenues estimated at more than 200 billion Euro is foreseen in the near future, by combining a highly viable and innovative fusion of three technological areas: microelectronics, chemistry and printing.[1] Smart use of metallic inks to render patterned structures conducting when deposited at polymer substrate-friendly temperatures (<150°C[2]), enables thin, light-weight and low-cost electronic devices. Potential applications are organic photovoltaics,[3, 4] transistors,[5] and radio frequency identification (RFID) tags.[6-8]

Metallic inks are often composed of precursor materials, including metallic nanoparticles (NPs) and metal-organic decomposition (MOD) inks. NP inks are formed by dispersing the NPs in aqueous or organic solvents by addition of colloidal stabilizers. Uniform and monodisperse NPs contribute thereby to a high colloidal stability and low electrical resistivity at low metallization temperatures.[9, 10] MOD inks, such as a Ag salt dissolved in a suitable solvent,[11] form NPs *in situ* upon destabilization during a solution step. NP inks usually have a higher metal loading than MOD inks and are more widely available commercially, and metal structures made from NP inks generally have a higher conductivity and contact resistances have been reported to be 5-10 times lower.[12] MOD inks do not require colloidal stabilizers and reduce nozzle clogging when used in inkjet printing, an often reported patterning technique for both inks.[9, 10, 13, 14] Writing a Ag NP ink with a rollerball pen on paper with a resolution down to 250 µm is probably the most simple and broadly accessible patterning technique reported in literature.[6]

Both types of ink require an additional sintering or decomposition step to render the precursor material conductive. Typically, heat is used to precipitate the metal and to burn off the organic ligand in MOD inks, or, in case of NP inks, to decompose the organic stabilizer. Compared to MOD

inks, NP inks often require higher annealing temperatures to decompose stabilizing agents and other polymeric additives that inhibit electrical conductivity.[11] Sintering typically requires >30 min process time and/or higher temperatures (>250°C) to form continuous metal structures, albeit percolating networks.[1] However, high sintering temperatures are incompatible with common low-cost polymer foils, such as poly(ethylene terephthalate) (PET) and polycarbonate (PC), that have a relatively low glass transition temperature. The choice of foil is therefore restricted to more expensive polymers such as polyimide (PI),[1] or the sintering temperature has to be drastically reduced. Lower sintering temperatures have been obtained by formulating an Ag ink with a low content of organic stabilizers. It revealed a conductivity of 5 - 65% of bulk Ag at a sintering temperature of 80°C, but the low content of binding materials made it hard to use in inkjet printing.[13] Very recently, an MOD ink was reported resulting in bulk conductivity of Ag after 15 min sintering at 90°C.[11] Although a very good conductivity was obtained in this study, the long sintering time makes it unsuited for high-throughput patterning in, for example, a roll-to-roll line.

Magdassi *et al.*[10, 15] reported recently a room temperature-sintering NP ink composed of Ag-poly(acrylic acid) (Ag PAA) NPs. This ink is destabilized by exchange of PAA for a halide, inducing not only the destabilization of the ink by detaching the PAA anchoring groups but also the coalescence of the Ag NPs, dramatically increasing the conductivity to approx. 10% of bulk Ag while the particle size increases from ~15 nm to 0.2-6 µm. The ink destabilizes and sinters in solution above a critical $Cl^-$ concentration of 50 mM. Addition of NaCl in a concentration below 50 mM to the aqueous dispersion of Ag-PAA NP ink resulted in room-temperature sintering upon solvent evaporation. A conductivity of up to 41% of that of bulk Ag was obtained by post-sintering inkjet-printed and dried Ag PAA NPs by a short (10 s) exposure to HCl vapor.

In this chapter, the compatibility of the fast and room temperature-sintering Ag-PAA NP ink is studied with three patterning strategies for low-

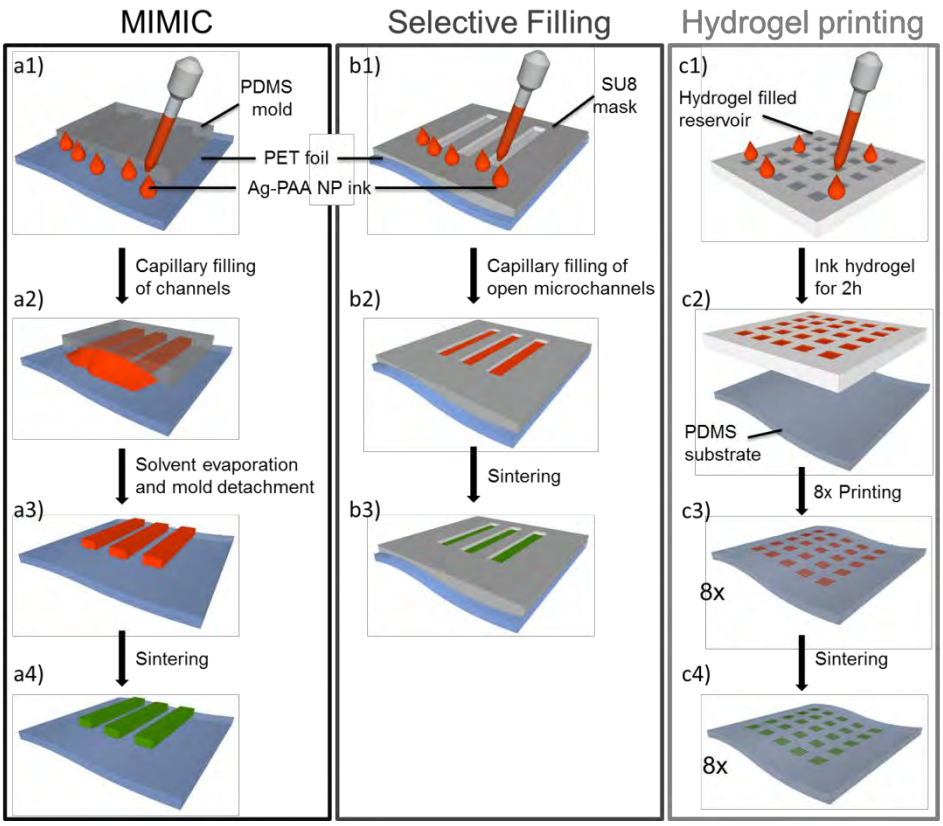
cost, large-area patterning on PET foil. Therefore, conductive Ag microwires have been patterned on PET foil by micromolding in capillaries (MIMIC), and Ag microwires have been embedded in a resist mask on PET foil by wetting-controlled deposition. Arrays of few-micron sized Ag dots have been deposited on an elastomeric substrate by the third patterning strategy, a hydrogel-based stamping device. Sizes of the structures and their conductivity after sintering are being assessed. Furthermore, a faster evaporating solvent for the Ag-PAA NP dispersion is evaluated and the effect of the layer thickness on sintering and the corresponding resistivity is studied.

## 7.2 Results and Discussion

Three patterning strategies have been deployed in this study (Scheme 7.1). In the first strategy (Scheme 7.1a), Ag microwires are formed on PET foil by patterning the Ag-PAA NP ink with MIMIC and subsequent sintering. Conformal contact of a patterned, elastomeric mold and PET foil, activated by short exposure to $O_2$ plasma, formed channels with two open ends on the PET foil. The mold for MIMIC was made by replica molding commercially available poly(dimethylsiloxane) (PDMS) against a patterned Si wafer. The channels were subsequently filled by placing a drop of Ag-PAA NP ink at one of the channel entrances (Scheme 7.1a1). The channels filled instantly upon capillary action (Scheme 7.1a2). The solvent was evaporated under a stream of $N_2$, whereafter the elastomer mold was peeled off, leaving the patterned Ag wires on the foil (Scheme 7.1a3). Sintering was induced by destabilization of the patterned Ag-PAA NPs by exposure to HCl vapor for 5 min (Scheme 7.1a4).

More interestingly in terms of a functional three-dimensional device are Ag features embedded in a chemically non-reactive and easily patternable mask. This is obtained by the second patterning strategy (Figure 7.1b). The Ag-PAA NP ink was placed at the entrance of the open microchannels by micropipetting (Scheme 7.1b1), whereafter the ink filled the open

microchannels within 5 s under capillary force (Scheme 7.1b2). Sintering of the Ag-PAA NPs was induced to form Ag wires embedded in SU8 (Scheme 7.1b3). To study an alternative patterning technique with the potential for high-resolution printing, which typically cannot be obtained with inkjet printing, Ag-PAA NPs were printed using a stamping device with hydrogel reservoirs to form arrays of Ag dots with a diameter of only a few microns (Figure 7.1c). The hydrogel was inked for ~2 h with 50 µL of Ag-PAA NPs dispersed in water (Scheme 7.1c2), allowing up to eight subsequent prints with reinking only once after four prints (Scheme 7.1c3). The printed Ag-PAA NP dots were sintered by exposure to HCl vapor (Scheme 7.1c4).




**Scheme 7.1** Schematic representation of the three studied patterning techniques: (a) Ag microwires are formed on top of PET by MIMIC; (b) Ag microwires are embedded in an SU8 resist mask on PET foil; (c) Few-micron-sized Ag dots are printed from a hydrogel reservoir onto a PDMS substrate.

### 7.2.1 Ag Wires on PET by MIMIC

Five millimeter long and 100 µm-wide, densely packed Ag-NP microwires were obtained over an area of 1 x 1 $cm^2$ on PET foil by MIMIC (Figure 7.1a-b), as was described above (Scheme 7.1a1-4). The open-end channels in PDMS (100 µm wide and spaced, 32 µm high) were filled with Ag-PAA NPs dispersed in water by capillary action. Complete solvent evaporation was established within approx. 1 h. The density of Ag NPs decreased towards the channel openings, which lead to interrupted and therefore non-conducting Ag agglomerations at the channel openings (Figure 7.1c-d).

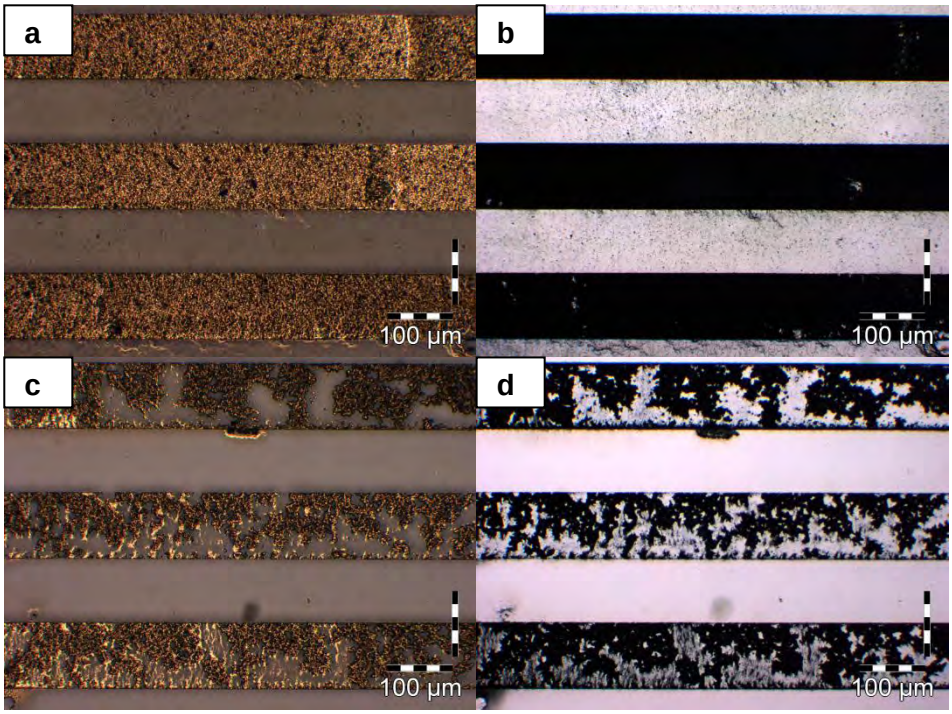



**Figure 7.1** Optical microscopy images in reflection (a, c) and transmission (b, d) mode in (a, b) the center of the MIMIC-patterned lines and (c, d) near the edges of the channels before sintering.

The electrical resistivity $\rho$ (in Ωm) of the sintered Ag microwires was determined according to equation (7.1), with $R$ (in Ω) being the electrical resistance, $A$ (in $m^2$) the cross-sectional area of the specimen and $l$ (in m) the wire length.

$$\rho = R\frac{A}{l} \tag{7.1}$$

The wire resistance $R$ over length $l$ was calculated by measuring the current $I$ (in A) as function of the applied voltage $V$ (in V) in a two-point probe measurement. Three height profiles on different points along the Ag wire were measured with profilometry and averaged, whereafter the area underneath the curve was integrated to obtain an averaged value for $A$ (Figure 7.2). The length of the wire was measured by optical microscopy.

**Figure 7.2** Cross-sectional profiles and their average at several positions of a Ag wire made by MIMIC and subsequent sintering.

From a measured resistance of 1.18 Ω over a wire length of 399 µm with a cross-sectional area of 60.4 ± 2.3 µm², a resistivity of 43 ± 19 µΩcm (average over three) with a minimum of 17.9 µΩcm was obtained for MIMIC-patterned, sintered Ag microwires on PET foil from aqueous Ag-PAA NPs. The larger deviation between the average and the best obtained resistivity can originate from a deviation in the layer thickness over the length of the three measured wires. The obtained resistivity is, with a minimal value of 17.9 µΩcm, roughly a factor 11 higher than the resistivity of bulk silver ($\rho_{bulk}$ = 1.59 µΩcm[16]). Although a factor 11 is already a good value for room temperature sintered Ag NPs, Grouchko *et al.*[15] reported a resistivity as low as 3.84 µΩcm (factor 2.4) for Ag structures, deposited by

inkjet printing, upon sintering in HCl vapor. Furthermore, a resistivity of 16 ± 2 μΩcm was reported for Ag wires (width 95 μm, thickness 500 nm) formed by inkjet printing of a self-sintering silver dispersion with low NaCl concentration ([NaCl] < 50 mM). In this system, the NaCl concentration increased to above the critical value of 50 mM simply by water evaporation, leading to particle destabilization and formation of a conducting silver network. The authors mentioned a low-density packing of the NPs as an explanation for the higher resistivity, as a result of the immediate coalescence of the NPs in the liquid thereby hindering any optimization of the packing. With HCl vapor as the sintering agent, the process of destabilization and packing of the particles is separated, allegedly leading to minimal distortion of the packing during sintering and a higher conductivity. According to this theory, non-optimal particle packing might be the reason for the higher resistivity obtained here. MIMIC might hinder an optimal particle packing in the channel, due to contact angle-dependent drag of the contact line at the channel sidewalls.

The self-sintering of the Ag-PAA NP ink with NaCl in a concentration below the critical value of 50 mM as reported by Grouchko *et al.*[15] was studied as well. Therefore, an aqueous Ag-PAA NP dispersion with 40 mM NaCl was patterned by MIMIC on PET as described before. Evaporation of the solvent (water) induced instant, room temperature sintering forming silvery-shining microwires. However, the sintering resulted in strong clustering of the particles, forming numerous non-connected grains. Two-point probe measurements confirmed the Ag wires to be disconnected as no conductance could be measured.

Water, as dispersing agent of the Ag-PAA NPs, was found to be not ideal to pattern Ag wires via MIMIC, as the evaporation was slow (1-2 h) and caused a drag of NPs out of the channel upon final evaporation. A faster evaporating, polar protic solvent that is suitable to pattern the Ag-PAA NPs with MIMIC was found to be methanol (MeOH).[16, 17] The NP dispersion in MeOH was stable for about one day, with an average particle size of 28 ± 13 nm 1 h after preparation (average particle size in water 21 ± 13 nm).

The fast evaporation of MeOH and partial uptake by the PDMS mold within ~15 s allowed several passes of dispensing and complete evaporation to increase the amount of Ag-PAA NPs in the channels. Centimeter long Ag wires have thus been obtained on PET (Figure 7.3) with a line edge roughness of ~1.2 µm. An average layer thickness of ~1.5 µm was obtained (Figure 7.4). Sintering was induced by 5 min exposure to HCl vapor at room temperature.

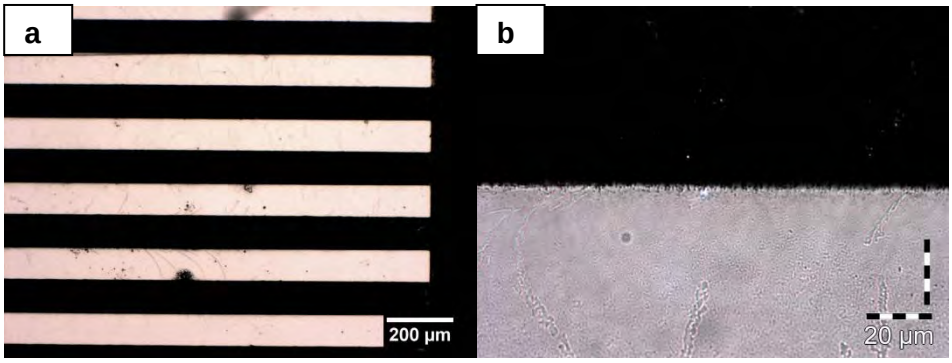



**Figure 7.3** Transmission microscopy images of (a, b) MIMIC-patterned Ag wires from Ag-PAA NPs dispensed in MeOH. (b) Magnified image of (a) showing the line edge roughness of the patterned wire.

**Figure 7.4** Cross-sectional profiles at several positions of a sintered Ag wire and their average.

From a measured resistance of 4.66 Ω over a wire length of 449 µm with a cross-sectional area of 148 ± 13 µm², a resistivity of 326 ± 110 µΩcm

(average over three) with a minimum of 154 μΩcm was calculated for MIMIC-patterned, sintered Ag microwires on PET foil from a Ag-PAA NP dispersion in MeOH. A very high resistivity of $1.3 \times 10^{10}$ μΩcm was measured before sintering. The evident transition in the resistivity before and after sintering shows clearly the effect of particle destabilization and sintering on the conductance of the wire. Before sintering, the packed Ag NPs are basically non-conducting. Sintering reduced the resistivity drastically, but it remained roughly a factor 8.5 higher than the value obtained from the aqueous dispersion. This relatively high resistivity has two possible reasons. The first one is particle packing: the chosen solvent, MeOH, did not stabilize the Ag-PAA NPs as good as water, leading to pre-coalescence and clustering in the dispersion. Most evidently, this was observed by the steady (but slow) separation of larger particle clusters from the dispersion. After about one day, most of the particles had precipitated. Additionally, the fast evaporation of MeOH might not provide sufficient time for optimal particle packing before complete solvent evaporation. The second reason for the observed low resistivity might be incomplete sintering. The cross-sectional area *A* was calculated on the assumption, that all Ag-PAA NPs in the trench were destabilized and therefore sintered. However, the HCl vapor introduced to destabilize the Ag-PAA NPs to form conductive Ag microwires, might have only induced sintering at the top surface of the ~1.5 μm thick microwire. The lower part of the filled channel is then shielded from the HCl vapor, leading to a potentially thick non-sintered and strongly non-conductive part of the Ag wire. Thus, the calculated value for *A* might not correspond to the sintered metallic cross section, consequently leading to a too high calculated resistivity.

The proposed incomplete sintering was further investigated by the fabrication of thinner (~529 ± 9 nm; Figure 7.5) Ag wires on PET. With a single run of MIMIC, the Ag-PAA NPs dispersed in MeOH did not form a connected wire. By two cycles of MIMIC and determination of their resistivity, an average resistivity of 1.2 ± 0.3 mΩcm (average over 4) with a

minimum of 1 mΩcm was obtained, from a measured resistance of 41 Ω over a wire length of 216 µm with a cross-sectional area of 53 µm.

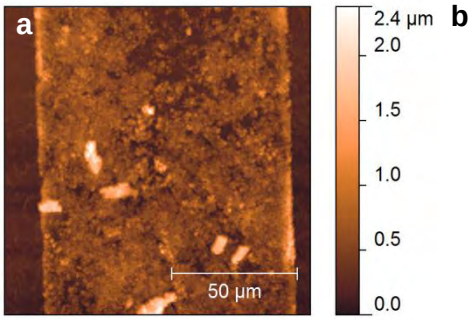



**Figure 7.5** (a) Atomic force microscopy image and (b) three cross-sectional profiles and their average of a sintered, MIMIC-patterned Ag wire on PET foil, formed from Ag-PAA NPs dispersed in MeOH.

For the thinner Ag wires, formed from Ag-PAA NPs dispersed in MeOH, an even higher resistivity was obtained when compared to the thicker wires. In first instance, this does not support the proposed, limited sintering depth. However, the more inhomogeneous layer thickness and the large amount of grain boundaries makes a fair comparison difficult. From the results, no conclusive effect of the sintering depth can be given for the NPs in MeOH, and more work is clearly needed to investigate this issue further.

## 7.2.2 Embedded Ag Wires on PET Foil

A method to make metal structures embedded in SU8 is described in Scheme 7.1b1-3. Hundred micron wide and spaced, 10 µm deep trenches are photolithographically patterned in an SU8 layer, after deposition on PET foil. The surface energy of SU8 was increased by a short $O_2$ plasma treatment, reducing the static contact angle of SU8 from 74.8 ± 1.5° to <5°, to improve the wetting by the aqueous Ag-PAA NP solution. The Ag-PAA NP ink filled the open microchannels within 5 s by capillary forces, after the ink was placed by micropipetting at the entrance of the open microchannels. After drying, the filling process was repeated to obtain a

thicker layer. Sintering resulted in embedded Ag wires on PET foil (Figure 7.6).

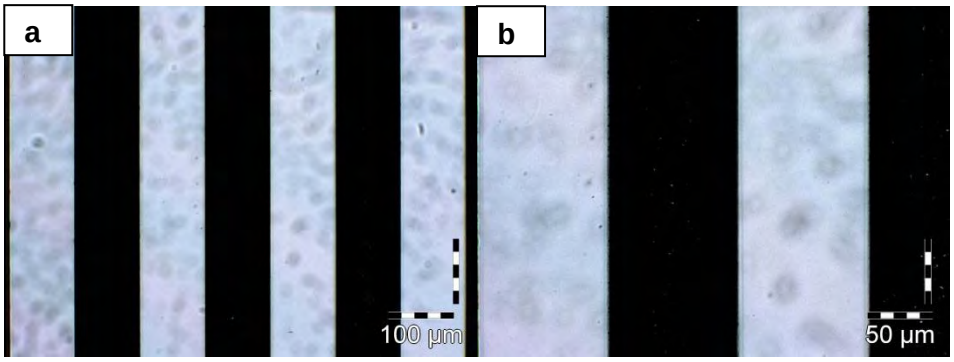



**Figure 7.6** Transmission microscopy images of (a, b) sintered Ag-wires formed in SU8 channels on PET foil from Ag-PAA NPs dispensed in water. (b) is a close-up of (a).

**Figure 7.7** Cross-sectional profiles at three positions of a sintered Ag wire and their average in black for a non-filled and filled microchannel.

From a measured resistance of 0.99 Ω over a wire length of 227 µm with a cross-sectional area of 237 ± 14 µm$^2$ (Figure 7.7), an average resistivity of 128 ± 22 µΩcm with a minimum of 103 µΩcm was obtained for the described patterning strategy with Ag-PAA NPs in water. The resistivity is much higher than the resistivity of 17.9 µΩcm obtained for MIMIC-patterned structures. As the aqueous dispersion is identical to the one used

in MIMIC patterning, poorer packing is unlikely to be the reason for this high value. Again, the limited conductivity might be attributed to incomplete sintering of the 2.5 μm thick Ag microwire. In addition to the previously MIMIC-patterned wire, only the top side of the embedded Ag-PAA NPs wires is exposed to HCl gas, the other sides are covered (protected) by the chemically resistant SU8.

The proposed deficiency in sintering depth was further investigated by the fabrication of thinner (~953 ± 14 nm) Ag wires in the channel by one time filling, and determination of their resistivity. From a measured resistance of 0.84 Ω over a wire length of 464 μm with a cross-sectional area of 64 μm , an average resistivity of 14.9 ± 3.7 μΩcm (average over 5) with a minimum of 11.6 μΩcm was obtained for Ag wires embedded in SU8 formed from an aqueous Ag-PAA NP dispersion. The much lower and excellent resistivity obtained for the thinner Ag wires embedded in the SU8 channels, only a factor ~7 higher than bulk silver, supports clearly the validity of the earlier proposed incomplete sintering in the 2.5 μm thick Ag wires. Furthermore, the value for the resistivity of these thinner lines is in between the values for the prematurely self-sintering and non-optimally packing Ag NP dispersion with incorporated NaCl (16 ± 2.2 μΩcm[15]) and the extremely low resistivity (3.84 μΩcm[15]) reported for the 500 nm thick, HCl-sintered Ag-PAA NPs. The here obtained low resistivity might actually be even lower than here reported, as a non-sintered area at the bottom of the 950 nm thick Ag-layer cannot be excluded.

To obtain a better insight in the actual sintering depth and the likeliness of a non-sintered core in the patterned Ag microwires leading to a too high calculated cross-sectional area and thus a high resistivity, a sintered layer thickness was calculated under assumption of the best possible resistivity. The lowest reported resistivity for the aqueous Ag-PAA NPs is 3.84 μΩcm.[15] With measured quantities for the resistance, wire length and width, and the best reported resistivity, an ideally expected layer thickness could be calculated from equation 7.1. The calculated, sintered layers were surprisingly thin. A sintered layer thickness of 130 nm was calculated for

the 604 nm thick, MIMIC-patterned Ag wire on PET. For the SU8-embedded Ag wires, conducting layer thicknesses of 88 nm and 212 nm were obtained for the 2.5 µm and 950 nm thick wires, respectively. While the first two values indicate a maximal sintering depth of around 100 nm, the thinner Ag microwire embedded in SU8 seems to be sintered twice as deep. It can also be interpreted as an indication for a sintering depth of ~100 nm in combination with an improved particle packing. Therefore, particle packing could be better in the open microchannels than with MIMIC. The calculated sintering depths of Ag wires, formed from Ag-PAA NPs dispersed in MeOH, are much less. Sintering depths of only 37 nm and 20 nm were calculated for the 1.5 µm and 529 nm thick wires, respectively. The very low calculated sintering depths are clearly different from structures made from the aqueous dispersion. It strongly points out the disadvantageous particle packing and size distribution as a result of the rather instable MeOH dispersion.

### 7.2.3 Sol-Gel Printed Ag Dots on an Elastomeric Surface

To study an alternative patterning technique with the potential for printing with a resolution not typically obtained by inkjet printing, Ag-PAA NPs in water were printed from hydrogel reservoirs in a stamping device to form arrays of Ag dots with a diameter of only a few microns.

Reservoirs have been made in Si by optical lithography and standard KOH etching techniques, fabricating 25 reservoirs each with 144 pores of 5 µm width and a 25 µm membrane, according to a procedure reported earlier by our group.[18] A hydrogel was functionalized in the reservoirs, forming an intertwined network with submicron porosity. The hydrogel facilitates ink uptake and transfer similar to a stamping pad. After inking the hydrogel for 2 h with a Ag-PAA NP solution, the stamping device was pressed against a freshly activated, unpatterned slab of PDMS. Up to eight sequential prints on different areas of the substrate with a total volume of 50 µL Ag-PAA NPs were performed, printing arrays of 144 Ag dots each (Figure 7.8).

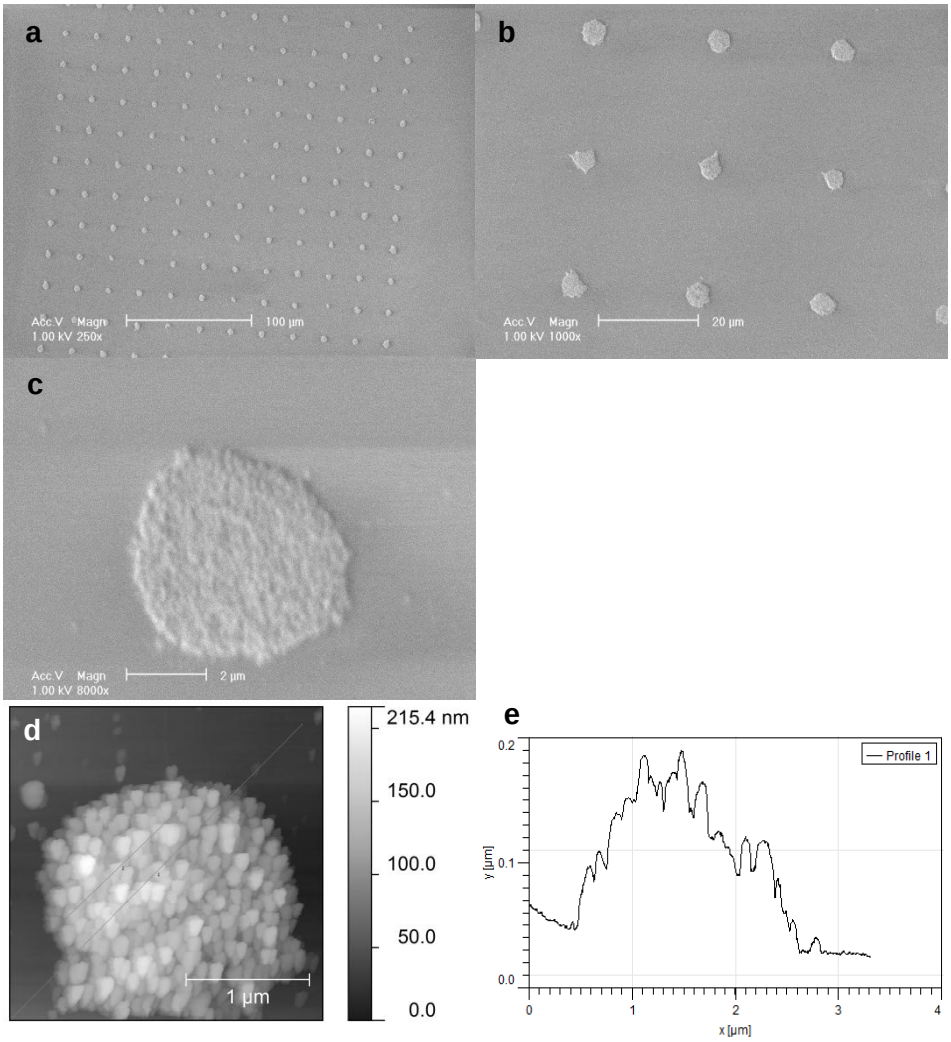



**Figure 7.8** Scanning electron (a-c) and atomic force microscopy image and profile (d, e) images of hydrogel-printed, non-sintered Ag-PAA dots on PDMS. (a) Array of 144 Ag dots with close-ups shown in (b) and (c). (d) AFM height image and (e) profile of an individual Ag dot.

The SEM images in Figure 7.8a-c display, with increasing magnification, one array of printed Ag dots on PDMS. Only one defect can be seen from the overview image in Figure 7.8a. The higher magnification in Figure 7.8b displays the irregular shape of the dots before sintering, and from the highest magnification image in Figure 7.8c a dot diameter of ~4.6 µm can be read out. From the AFM image of a different, smaller printed dot in

Figure 7.8d, an average height distribution of 97.7 nm and a root mean square (rms) roughness of 26.5 nm can be extracted. The height profile in Figure 7.8e shows a dot width of around 2 μm and gives an impression of the overall height distribution and roughness of a printed Ag dot.

Further analysis of the feature height and overall surface roughness was performed by measuring twenty individual, sintered Ag dots of a printed array with AFM. An average height of 266 nm with a relatively small standard deviation of ~12% over 20 printed dots was obtained. From the maximal height difference of 474 nm from the highest (average maximum height 579 ± 108 nm) to the lowest point per dot (average minimal height 105 ± 24 nm), a non-flat top side can be concluded. This is supported by the AFM profile in Figure 7.8e. From the average projected area (in average 6.8 ± 1.0 nm), and under the assumption of a circular shape, an average diameter of 3 μm was calculated. The average diameter value fits nicely in between the larger 4.6 μm dot from the SEM images and 2 μm of the AFM images.

SEM imaging (data not shown) of all eight sequential prints on PDMS showed a decrease in feature size and an increasing number of defectively printed dots per array (up to 17 defects over 144 dots in one array). Counted as defectively printed were all missing or very small (<1.2 μm) Ag dots. For every print, the width of 20 dots was measured from the SEM images and averaged, showing a steady decrease from 5.7 ± 1.3 μm to 3.5 ± 0.6 μm. The increase in defects and decrease of the printed dot size can originate from two factors: ink depletion and clogging. During printing, the hydrogel turned slowly silvery grey; an indication for sintering of the Ag-PAA NPs. Furthermore, no increase in feature size was observed after reinking the hydrogel after the fourth print, which would be expected for ink depletion. Therefore, clogging of the fine pores caused by particle sintering is the most likely cause for the decreasing printing quality.

These results demonstrate the utilization of the hydrogel stamping device to print Ag dots from an Ag NP dispersion at a few-micron scale. The

hydrogel allows to combine the qualities of spotting with the high resolution of microcontact printing. In average, Ag dots of 5.7 ± 1.3 µm have been printed on PDMS in eight sequential prints, with reinking after the fourth print. With a continuous printing technique, or a denser array, Ag droplets might be able to merge before solvent evaporation and form conductive lines or features, offering a whole new dimension to the patterning of room temperature-sintering particles.

## 7.3 Conclusions

In summary, silver wires have been patterned on PET foil by MIMIC, and silver wires embedded in SU8 have been fabricated on PET foil by wetting-controlled deposition in open microchannels. One hundred µm-wide Ag microwires with a length of 5 – 15 mm and a height of 0.6 – 2.5 µm have been fabricated. The influence of the solvent on the resistivity was studied by replacing water for MeOH in the Ag-PAA NP dispersion. The MIMIC process was sped up with MeOH as the solvent, and the layer thickness could be increased by multiple cycles of MIMIC. However, the MeOH dispersion was only semi-stable for a maximum of one day and resulted in higher resistivities as a result of non-optimal particle packing and pre-coalescence of the NPs in solution. Sintering was in most cases performed with HCl vapor. The self-sintering aqueous Ag-PAA NP dispersion with NaCl in a concentration below 50 mM, did not result in a continuous pattern. As a result, only interrupted and non-conducting Ag wires could be fabricated on PET foil with this self-sintering ink. Furthermore, a layer thickness dependency was found for the resistivity. Thicker layers showed a higher resistivity than thinner lines. This is attributed to incomplete sintering of the Ag wires, due to a blocked penetration of the HCl vapor into the bulk material after sintering of the top layer. As a result, the calculated values for the cross-sectional area $A$ in equation 7.1 were typically set too high, leading to calculated resistivities higher than those most likely occurring in the well-sintered top layer. Additionally, particle packing in

the channel might be less optimal with MIMIC, due to contact angle-dependent drag of the contact line to the channel sidewalls.

With Ag-PAA NP-loaded hydrogel reservoirs, arrays of 144 Ag dots each have been repetitively printed on PDMS in eight sequential prints. From a statistical study over 20 sintered dots, average diameter and height were determined to be approx. 3 µm and 266 nm, respectively. The submicron porosity of the hydrogel allowed a critical control over ink uptake and release. A growing number of defects was found, in the sense of non-printed or very small dots, upon increased print number. Up to 17 defects, out of 144 dots, were counted for the eighth print.

The here utilized, room temperature-sintering Ag-PAA NPs have an enormous potential and compatibility for flexible electronics. Other Ag NP formulations require high annealing temperatures up to 320°C for up to 30 min,[13] to obtain conductivities in the here reported range. Although we did not obtain the 41% conductivity reported by Grouchko *et al.*,[15] a factor 7.3 lower conductivity than bulk Ag is a very good result. The resistivity might be even decreased further, by reduction of the layer thickness or by ensuring full layer sintering by other particle destabilizing reactions.

## 7.4 Experimental Section

### 7.4.1 Ag NP Synthesis

Silver nanoparticles were synthesized by the reduction of silver acetate with ascorbic acid in the presence of poly(acrylic acid) sodium salt ($M_w$=8000), similar to the procedure reported by Magdassi *et al.*[10] In short, 2.25 g silver acetate (Acros) and 0.934 g of 45 wt% poly(acrylic acid) sodium salt ($M_W$ 8000, Aldrich) were mixed and heated to 95°C for 15 min in 14 mL of MilliQ water. Then, 1.7 g of 30 wt% *L*-ascorbic acid (Aldrich) was slowly added, and the mixture was stirred for 30 min while heating. The obtained nanoparticles were washed by centrifugation, and the

obtained sediment was redispersed in MilliQ water. The pH of the dispersion was adjusted to 9.5 by the addition of 2-amino-2-methyl-1-propanol 95% (Aldrich). Directly before use, the dispersion was sonicated for 5 min. The Ag-PAA NPs were found to be very stable in water. The particle size was determined by dynamic light scattering to be 21 ± 13 nm (number average over five measurements) after half a year storage in a fridge. The Ag-PAA NP dispersion in MeOH was prepared by evaporating the water from 200 µL of the aqueous dispersion at 60°C in an oven. The dried particles were redispersed in 200 µL MeOH and sonicated for 5 min. After sedimentation of a few large particles, the supernatant was used as the ink.

### 7.4.2 Ag NP Sintering

Room temperature sintering of the patterned Ag-PAA NPs was induced by exposing the sample for 5 min at a distance of ~2 cm to a 37% HCl solution.

### 7.4.3 Preparation of PDMS Molds

The mold material, Sylgard-184 poly(dimethyl siloxane) (PDMS), was purchased from Dow Corning. PDMS molds were prepared by mixing the curing agent and the prepolymer manually in 1:10 volume ratio and curing overnight at 60°C against a photolithographically patterned Si master. After curing. The PDMS molds were peeled off from the Si wafer.

### 7.4.4 Preparation of SU8 Trenches on PET

Trenches in SU8-5 of 100 µm width and 9 µm depth have been prepared by standard photolithographic patterning on 200 µm thick PET foil (Kodak). For achieving an improved adhesion, PET was exposed to $O_2$ plasma for 1 min using a Tepla 300 UCL at 300 W. SU8-5 (MicroChem) was deposited on the activated PET foil by spincoating for 10 s at 500 rpm and 30 s at 1500 rpm, followed by a soft bake program starting at 25°C, holding the temperature at 50°C for 1 min, at 65°C for 1 min, and at 95°C for an additional 3 min after which the temperature was slowly decreased to

25°C. With a mask aligner (EVG620), the SU8 was exposed for 13 s at a proximity of 20 µm. A post-exposure bake starting at 25°C, holding the temperature at 50°C for 1 min, at 65°C for 1 min, and at 80°C for an additional 2 min after which the temperature was slowly decreased to 25°C, was followed by 90 s development in RER600, rinsing with isopropanol and blow drying by $N_2$.

### 7.4.5 Hydrogel Stamps

A Si stamping device with hydrogel reservoirs was fabricated according to literature.[18] In short, a chip with 25 reservoirs, each holding 144 pores of 5 µm width and a 25 µm membrane, was fabricated with standard photolithography patterning and KOH etching of a silicon-on-insulator (SOI) wafer. The chips were cleaned in Piranha solution (3:1 mixture of conc. sulfuric acid and 30% hydrogen peroxide. CAUTION! Piranha solutions should be handled with great care in open containers in a fume hood. Piranha is highly corrosive, toxic and potentially explosive) for 30 min and subsequently rinsed with MilliQ water, ethanol and then blown dry with $N_2$. The chip was functionalized with 1H,1H,2H,2H-perfluorodecyltrichlorosilane (PFDTS) (ABCR) overnight. By exposure to $O_2$ plasma, PFDTS was removed from the chip except for the printing side of the chip. The inner walls of the reservoir were functionalized and the pores filled with a hydrogel.[18] As initiator, ammoniumpersulfate and tetramethylethylenediamine were added under Ar atmosphere. The hydrogel-filled reservoirs were kept under water until use.

To print with the hydrogel reservoirs, 5-10 µL of Ag-PAA NPs dispersion was micro-pipetted on the reservoirs and left for ~2 h, allowing the ink to penetrate the hydrogel. Just before printing, excess ink was removed and the loaded chip was gently pressed against UV/$O_3$-activated PDMS. After a few seconds, the chip was gently removed.

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# Summary and Outlook

The alternative patterning strategies developed in this thesis offer new lithographic routes to the fabrication of flexible electronic devices on polymeric foils. Main aim of the research has been the development of a patterning strategy solely based on nanoimprint lithography (NIL), for the fabrication of a complex, flexible electronic device. More specifically, a flexible bottom-contact, bottom-gate thin-film transistor (TFT) was made on poly(ethylene naphthalate) (PEN) foil. The explicit challenges with patterning on foil were its temperature sensitivity and its mechanical and in-plane instability.

Wavy substrates resulted in inhomogeneous and generally thick residual layers, which could not be removed completely by reactive ion etching. Either a residual layer remained in the wave valleys, or the resist mask was removed on the wave hills upon prolonged etching. Thus, patterning and process strategies had to be developed for thermal and UV NIL to control the residual layer thickness and its complete removal. Furthermore, transistor materials (e.g. dielectric) were evaluated and the patterning process was adjusted to meet the materials compatibility. To reduce the waviness and improve the stability of the foil, the foil was temporarily bonded to a supporting carrier. The process to fabricate these foil-on-carriers (FOCs) was continuously improved during this research to reduce the bending radius and in-plane waviness, providing a mechanically stable platform for proper processing. Complete removal of the residual layer on foil was finally obtained for thermal NIL by introducing a second, more etch-resistant resist with double-layer NIL (dlNIL) (Chapter 3), which

serves as an etch mask for the underlying resist. For step-and-flash imprint lithography (SFIL) of the common-gate flexible TFTs (Chapter 4), the optimized, thermally flat imprinted FOC provided sufficient control over the residual layer. For multistep SFIL of the fully patterned flexible TFTs (Chapter 5), however, the flatness of the original FOC was insufficient to allow multistep imprinting. Therefore, imprint planarization was introduced to provide a flat plateau on the foil, allowing a sufficient control and complete removal of the residual layers of all three subsequently imprinted layers.

Exact alignment of source-drain and gate features of a TFT is required to minimize their overlap and reduce parasitic effects. However, precise alignment in a large-area and high-throughput roll-to-roll (R2R) process is economically and eventually even technologically not feasible. A self-aligned process is thus needed. Reports have shown self-aligned flexible TFTs made by imprinting a three-dimensional mask containing all layer information, or using the gate as a photomask to define the source-drain layer in a subsequent process step. In this thesis (Chapters 6 and 7), solution-based deposition strategies to form metallic structures on foil at room temperature have been studied, with the aim to assess their suitability for large-area processing. Copper and silver wires were formed on PET foil by directing metal precursor inks into microchannels under the influence of capillary forces. The metal precursors were subsequently sintered at room temperature to form silver, or utilized to form copper by electroless deposition.

Chapter 1 provides a general introduction to this thesis. Chapter 2 reviews the historical development of the more traditional, large-area printing techniques for the fabrication of flexible electronics to alternative, high-resolution patterning strategies such as soft and nanoimprint lithography. The benefits and limitations of each of the patterning techniques are discussed, as well as the challenges for processing on mechanically instable and temperature-sensitive foils. Challenges are to be solved in materials

and processes with the perspective for the economically feasible low-cost, high-throughput fabrication of flexible electronic devices.

Chapter 3 introduces a thermal imprint process capable of simultaneously patterning structures over a large dimensional range on Si and polymeric foil, from the submicron to the millimeter scale. The imprint and filling quality of this double-layer NIL process was compared with regular NIL and reverse NIL. dlNIL allows the combination of resists for tailored nanostructure fabrication. As an example, two resists with a difference in etch resistivity have been combined, allowing the complete removal of an inhomogeneous residual layer on foil.

Chapter 4 shows the fabrication of flexible TFTs on PEN foil, with only the source-drain layer patterned by SFIL. A foil-on-carrier system has been introduced to reversibly glue the foil to a Si carrier, enhancing the dimensional stability and flatness of the foil to result in a thinner and more homogeneously distributed residual layer thickness. The obtained performance of the TFT devices, showing a mobility of $\mu = 0.56$ $cm^2V^{-1}s^{-1}$ with an on/off ratio of $>10^7$ and near-zero threshold voltage, was found to be in good agreement with similar, photolithographically patterned state-of-the-art devices.

Chapter 5 presents a multistep imprinting process for the fabrication of bottom-contact, bottom-gate TFTs on Si and PEN foil with all three layers of the metal-insulator-metal (MIM) stack patterned by SFIL. A novel, SFIL-patterned planarization layer was introduced on FOC, in order to enhance the flatness of the foil and thus to result in a thinner and more homogeneous residual layer. Two oxides and three organic materials have been tested as a dielectric, of which only $SiO_2$ provided the necessary performance. TFTs with channel lengths from 5 μm down to 250 nm were fabricated on Si and PEN foil, showing channel length-dependent charge carrier mobilities, μ, in the range of 0.06 - 0.92 $cm^2V^{-1}s^{-1}$ on Si and of 0.16 - 0.56 $cm^2V^{-1}s^{-1}$ on PEN foil. The performance of the TFTs on Si and PEN foil with the largest channel length (5 μm) is comparable with state-of-the-art

devices fabricated by photolithographic patterning. Scaling of the channel length from 5 µm down to 500 nm showed a transition in the mobility at 1.5 µm, from semi-constant at higher to decreasing for smaller channel lengths. The smallest channel of 500 nm, unprecedented in literature, showed a good saturation mobility of 0.18 $cm^2V^{-1}s^{-1}$.

Chapter 6 describes the selective deposition of materials from solution in open microchannels, patterned in SU8 by embossing on poly(ethylene terephthalate) (PET) foil. The filling mechanism was studied first using a fluorescent dye, showing a feature width dependence. The solute was deposited over the entire width of the channel for narrow (1-2 µm) features, while the solute was only deposited at the channel edges for wider (5-20 µm) features. Therefore, a capillary assembly mechanism has been proposed, which is identified by a contact angle-dependent solute deposition as a result of a changing effective radius of the U-shaped meniscus. Metallic microwires were fabricated in the open microchannels by selective deposition of Pd salts as the precursor for Pd NPs, serving as a catalyst for electroless deposition of Cu from solution.

Chapter 7 shows the applicability of room temperature-sintering poly(acrylic acid)-capped Ag nanoparticles (Ag-PAA NPs) to create metallic silver structures by a range of micro/nanofabrication methods. Silver wires were patterned on PET foil by micromolding in capillaries (MIMIC), and silver wires embedded in SU8 were fabricated on PET foil by wetting-controlled deposition in open microchannels. One hundred µm-wide Ag microwires with a length of 5 – 15 mm and a height of 0.6 – 2.5 µm were obtained, showing a maximum conductivity of only a factor 7.3 lower than bulk silver. Furthermore, a limit of around 100 nm of the sintered depth was observed when sintering by HCl vapor. Thus, the bulk of the patterned wires was not sintered and remained non-conductive. Methanol was studied as an alternative dispersing solvent. It allowed faster patterning by MIMIC, but resulted in a high resistivity due to a low particle packing quality and pre-coalescence in solution. NaCl in a concentration below 50 mM was studied to induce self-sintering upon water evaporation, as an

alternative sintering agent for HCl. NaCl-induced sintering led to sintered, but non-connected clusters of Ag in the channel. The feasibility of the Ag-PAA NP ink for repetitive printing of 3 μm-wide Ag dots with a hydrogel reservoir stamping system was studied as an alternative printing technique. Arrays of 144 Ag dots each were printed up to eight times on a poly(dimethyl siloxane) (PDMS) substrate, with up to 17 defects in the eighth print as a result of clogging of the channels of the stamping device.

Some general lessons can be drawn from the results described in this thesis. Thermal NIL (Chapter 3) suffers from thermal expansion mismatches and the heat sensitivity of the foils, making thermal NIL rather unfavorable to pattern multilayered electronic devices. The good electrical performance and submicron channel lengths of the flexible TFTs, patterned exclusively with UV NIL as presented in Chapters 4 and 5, demonstrate the quality of room-temperature NIL-patterned electronic devices. However, the enormous and continuous effort in this thesis undertaken to improve the mechanical stability and flatness of the foil by changing the FOC system, adding additional resist masks or planarization layers, demonstrates also the difficulties of obtaining a reproducible NIL patterning process over the wide dimensional range of submicron to millimeter scale. The critical overlay of the source-drain and gate layers demands the development of a self-aligned imprint process, in order to be able to integrate the process in high-throughput and high-resolution R2R lines to fabricate low-cost, high-quality flexible electronics for the consumer market. The fabrication lessons learned here for the room-temperature, low-pressure and high-precision technique SFIL, are being implemented in a self-aligned R2R patterning strategy. As an example, the importance of critical control over the foil and the residual layer has been stressed, and tentative solutions such as an imprinted planarization layer or masking resist have been given. Furthermore, the choice of the device materials and the compatibility with the individual process steps was verified and further adjusted where necessary.

The demonstrated, self-aligned fabrication of metallic microwires in open microchannels on PET in Chapters 6 and 7 shows a solution-based route for low-cost and high-throughput patterning on foil, which is promising for R2R integration. Especially the utilization of the room temperature-sintering Ag-PAA NPs with a near-bulk conductivity is promising for future fast and large-area patterning strategies. However, more research is required to study the dimensional limitations of both patterning strategies. In direct comparison, Pd-catalyzed electroless deposition of copper is less controllable and specific, forming more irregular shapes and feature heights. The ease of patterning thin but very conductive silver wires from a long-term stable aqueous solution allows integration in a R2R line to pattern the metallic contacts of a flexible electronic device. A possible, solution-based route can thus be imagined in which all patterning techniques studied in this thesis are integrated into a low-cost, high-throughput fabrication process for flexible electronic devices. A guide map that directs the metallic precursor materials (or polymers) to the right positions should be incorporated in the topography of a three-dimensionally, UV NIL-patterned device layout, in order to form the individual parts of the device. Such fabrication methods will be the strategies for future generations of flexible electronic devices.

# Samenvatting en vooruitblik

De in dit proefschrift ontwikkelde, alternatieve patroneringstechnieken bieden nieuwe lithografische routes om flexibele elektronica op polymere folies te fabriceren. Hoofddoel van het onderzoek was de ontwikkeling van een enkel op nanoimprint-lithografie (NIL) gebaseerde patroneringsstrategie om flexibele elektronica te fabriceren. Meer specifiek zijn dunne-film-transistoren (TFT's) met een onderliggende gate op flexibele poly(ethyleen-naftalaat)- (PEN-) folie gemaakt. Expliciete uitdagingen bij het patroneren op goedkope folie zijn de temperatuurgevoeligheid en de mechanische instabiliteit van de folie.

Golvende substraten leidden tot inhomogene en dikke restlagen van resist, die niet in zijn geheel d.m.v. droog-etsen (RIE) verwijderd konden worden. De restlaag van resist bleef achter in de dalen van het golvende substraat of de gepatroneerde resistlaag werd op de toppen ongewild verwijderd door overetsen. Aldus, moesten patroneer- en processtrategieën voor thermisch en UV NIL worden ontwikkeld, die voldoende controle konden bieden over de dikte van de restlaag en de complete verwijdering ervan. Verder zijn verschillende transistormaterialen (bijv. het diëlectricum) geëvalueerd en is het patroneringsproces waar nodig op deze materialen aangepast. De golving en de mechanische stabiliteit van de folie zijn verbeterd door deze tijdelijk op een drager te plakken. Deze folie-op-dragers (*foil-on-carrier*; FOC) zijn gedurende het onderzoek steeds verder verbeterd met betrekking tot hun kromming en stabiliteit. Zij boden uiteindelijk een toereikend mechanisch stabiel platform. De introductie van een tweede, meer etsresistente resistlaag bovenop de eerste resistlaag in dubbellaags

NIL (dlNIL) resulteerde in de volledige verwijdering van de restlaag in thermisch NIL op folie. De resultaten hiervan zijn in hoofdstuk 3 besproken. Voor het patroneren van TFT's met een algemene gate d.m.v. *step-and-flash imprint lithography* (SFIL) werden de FOC's verder geoptimaliseerd door ze thermisch vlak te persen (hoofdstuk 4). Deze verbetering van de FOC's was helaas niet afdoende om volledig gepatroneerde, flexibele TFT's in een multistaps SFIL-proces te maken (hoofdstuk 5). Om dit op te lossen werd een imprint-egaliseringsmethode ontwikkeld, om zo een vlak plateau op de folie te creëren. Hiermee kon de restlaag goed gecontroleerd en verwijderd worden in alle drie achtereenvolgend geïmprinte lagen.

In een TFT moeten source-drain en gate precies uitgelijnd zijn om hun overlap en daarmee ook parasitaire effecten te minimaliseren. Precies uitlijnen in een rol-tot-rol- (R2R-) proces over grote oppervlakken met een grote verwerkingscapaciteit is echter economisch en eventueel zelfs technisch niet haalbaar. Een zichzelf uitlijnend proces biedt dan uitkomst. Enkele voorbeelden van zelf-uitlijnende systemen om flexibele TFT's middels imprinten te maken zijn beschreven in de literatuur. O.a. kan een driedimensionaal masker met alle structuuraanwijzingen geïmprint worden, of een geïmprinte gate kan als fotomasker dienen om de posities van source en drain vast te leggen. In hoofdstukken 6 en 7 van dit proefschrift zijn depositietechnieken uit oplossing onderzocht en hun grootschalige toepasbaarheid voor het patroneren van metaalstructuren op folie bij kamertemperatuur. Door het sturen van metaaldepositie-initiërende inkt in microkanalen, onder invloed van capillaire krachten, konden koper- en zilverdraden op poly(ethyleen-tereftalaat)- (PET-) folie worden gevormd. De metaaldepositie-initiërende materialen werden vervolgens gesinterd bij kamertemperatuur om zilverdraden te vormen of gebruikt om koper vanuit oplossing af te zetten.

Hoofdstuk 1 geeft een algemene inleiding tot dit proefschrift. In hoofdstuk 2 wordt de historische ontwikkeling van alternatieve, hoge-resolutie-patroneringsstrategieën (zoals zachte- en nanoimprint lithografie) uit de

meer klassieke druktechnieken met grote verwerkingscapaciteit beschreven. Voordelen, nadelen en beperkingen van de individuele patroneringstechnieken en uitdagingen met betrekking tot de mechanisch instabiele en temperatuurgevoelige folies zijn besproken. Materialen en processen dienen daarbij altijd zo gekozen en ontwikkeld te worden, dat ze in een economisch haalbaar, goedkoop fabricageproces voor flexibele elektronica gebruikt kunnen worden.

In hoofdstuk 3 is een thermisch imprintproces geïntroduceerd dat in één keer patronen over een grote lengteschaal, van submicrometer tot millimeter, op Si en kunststof folie kan aanbrengen. De imprint- en vulkwaliteit van dit dlNIL-proces zijn vergeleken met regulier NIL en *reverse* NIL (rNIL). dlNIL maakt de combinatie van verschillende resists mogelijk voor een toegesneden fabricage van nanostructuren. Als voorbeeld zijn twee resists met een verschil in etsweerstand gecombineerd, die de volledige verwijdering van een inhomogene restlaag op folie mogelijk maakten.

Hoofdstuk 4 toont de fabricage van flexibele TFT's op PEN-folie, waarvan enkel de source-drain-laag gepatroneerd is met SFIL. Een FOC-systeem is geïntroduceerd om de folie tijdelijk op een drager te plakken, hetgeen de stabiliteit en golving van de folie ten goede komt en in een dunnere en homogenere verdeling van de restdiktes resulteert. De prestaties van de verkregen TFT's zijn in goede overeenstemming met vergelijkbare TFT's, die volgens de nieuwste stand der techniek d.m.v. fotolithografie gemaakt zijn. Een mobiliteit van $\mu = 0.56\ cm^2V^{-1}s^{-1}$, een aan/uit-verhouding van $>10^7$ en een drempelspanning van nagenoeg nul zijn behaald.

Volledig met SFIL gepatroneerde TFT's met een onderliggende gate en contacten die onder de halfgeleiderlaag liggen zijn op Si en PEN-folie gemaakt. Zij worden beschreven in hoofdstuk 5. De golving van de folie op de FOC is m.b.v. een nieuwe, SFIL-bereide egaliseringslaag gereduceerd, waardoor een dunne en homogene restlaag gecreëerd is. Twee oxides en drie organische materialen zijn getest als diëlectricum, waarvan alleen $SiO_2$

de vereiste kwaliteiten vertoonde. TFT's met een kanaallengte van 5 µm tot 250 nm zijn gemaakt op Si en tot 500 nm op PEN-folie. Deze gaven een mobiliteit, afhankelijk van kanaallengte en gatespanning, in de orde van 0.06-0.92 $cm^2V^{-1}s^{-1}$ op Si en 0.16-0.56 $cm^2V^{-1}s^{-1}$ op PEN-folie. De prestaties van de TFT's op Si en PEN-folie met een kanaallengte van 5 µm zijn vergelijkbaar met fotolithografisch gepatroneerde TFT's, die volgens de nieuwste stand der techniek gemaakt zijn. Bij het geleidelijk verkleinen van de kanaallengte van 5 µm naar 500 nm is een overgang te zien bij 1.5 µm, van vrijwel constant voor grotere kanaallengtes naar afnemend voor kleinere. Voor het kortste kanaal op folie van 500 nm werd een goede verzadigingsmobiliteit van 0.18 $cm^2V^{-1}s^{-1}$ gemeten.

Hoofdstuk 6 beschrijft de selectieve depositie van materiaal uit oplossing in open microkanalen, gemaakt van SU8, op PET-folie. Met behulp van een fluorescerende kleurstof werd het vulmechanisme onderzocht. De opgeloste stof werd over de hele kanaalbreedte gedeponeerd wanneer smalle kanalen (1-2 µm) gebruikt werden, maar alleen aan de randen in het geval van bredere (5-20 µm) structuren. De observatie van een contacthoek-afhankelijke materiaalafzetting door een veranderende effectieve straal van de U-vormige meniscus duidt op een capillair assemblagemechanisme. Metallische microdraden zijn in open microkanalen gevormd door selectieve depositie van Pd-zouten, die vervolgens als precursor voor Pd-nanodeeltjes dienden. De nanodeeltjes zelf zorgden op hun beurt voor de katalytische afzetting van koper uit oplossing.

In hoofdstuk 7 is de toepasbaarheid van polyacrylzuur-gefunctionaliseerde Ag-nanodeeltjes (Ag-PAA nanodeeltjes) onderzocht om metallische zilverstructuren te vormen bij kamertemperatuur met een reeks van micro- en nanofabricagemethoden. Zilverdraden zijn op PET-folie gevormd d.m.v. *micromolding in capillaries* (MIMIC). In een masker van SU8 ingebedde zilverdraden zijn gemaakt op PET-folie door oppervlaktespanning-gecontroleerde depositie in open microkanalen. Honderd micrometer brede zilverdraden met een lengte van 5 – 15 mm en

een hoogte van 0.6 – 2.5 μm vertoonden een maximale geleiding die slechts een factor 7.3 lager lag dan die van bulk zilver. Verder werd een limiet in de sinterdiepte van rond de 100 nm gevonden indien met HCl-gas gesinterd werd. Het merendeel van de gepatroneerde draad werd dus niet gesinterd en bleef daardoor isolerend. Als alternatief oplosmiddel werd methanol onderzocht. Patroneren d.m.v. MIMIC verliep sneller, maar de gemeten weerstand was hoger als gevolg van een kwalitatief mindere pakking van de deeltjes en het prematuur aggregeren van de deeltjes in de oplossing. NaCl werd als alternatief voor HCl in een concentratie onder de 50 mM toegevoegd aan de waterige dispersie om sinteren te induceren. Door het verdampen van water werd de kritische chloride-concentratie overschreden hetgeen sinteren tot gevolg had. NaCl leidde weliswaar tot sinteren, maar meer dan een open netwerk van zilverclusters kon niet worden gevormd in de kanalen. De toepasbaarheid van de Ag-PAA-nanodeeltjes-inkt is verder onderzocht met een alternatieve druktechniek. Hierin zijn 3 μm brede Ag-stippen herhaaldelijk op een polydimethylsiloxaan- (PDMS-) substraat opgebracht m.b.v. een stempelsysteem dat een hydrogel-inktreservoir bevat. Series van elk 144 Ag-stippen konden tot acht keer toe opgebracht worden. Een maximum van 17 defecten werd in de achtste opdruk geconstateerd als gevolg van aggregatie in de kanalen van het stempelapparaat.

Enkele algemene conclusies kunnen worden geformuleerd aan de hand van de in dit proefschrift behaalde resultaten. Zo zijn de verschillen in thermische expansie en de temperatuurgevoeligheid van de folie niet bevorderlijk voor het met thermisch NIL patroneren van elektronica die uit meerdere lagen opgebouwd is (hoofdstuk 3). De goede elektrische eigenschappen van de geheel met SFIL gepatroneerde, flexibele TFT's tonen de kwaliteit van de met NIL gepatroneerde, flexibele elektronica aan (hoofdstukken 4 en 5). De enorme en voortdurende inspanningen beschreven in dit proefschrift om de mechanische stabiliteit en vlakheid van de folie te verbeteren, laat echter ook zien hoe moeilijk het is om een reproduceerbaar NIL-proces te ontwikkelen. Door het veranderen van de FOC's of het toevoegen van extra resistmaskers of egaliseringslagen kon

over een grote lengteschaal (van submicron tot millimeter) worden gepatroneerd. Om voor de consumentenmarkt goedkope, kwalitatief hoogwaardige en flexibele elektronica te maken met een R2R-fabricagelijn, moet een zelf-uitlijnend proces ontwikkeld worden dat het kritische uitlijnen van de source-drain- en gate-lagen vervangt. De hier voor SFIL geleerde fabricagelessen kunnen in een zelf-uitlijnende R2R-patroneringsmethode geïmplementeerd worden. Als voorbeeld is de nadruk op de kritische controle over de folie en de restlaag gelegd en zijn mogelijke oplossingen zoals een geïmprinte egaliseringslaag of een extra resistmasker gegeven. Verder zijn de materiaalkeuze en de compatibiliteit met de individuele processtappen geverifieerd en waar nodig aangepast.

In hoofdstukken 6 en 7 werd een oplossingsgebaseerde route uitgewerkt om op een goedkope manier grote hoeveelheden van metallische microdraden in open microkanalen op PET te fabriceren. Dit is veelbelovend voor de integratie in een R2R-fabricagelijn. Vooral de toepassing van de op kamertemperatuur-sinterende Ag-PAA-nanodeeltjes met nagenoeg dezelfde geleiding als bulk zilver zijn veelbelovend voor toekomstige, snelle patroneringsmethoden over grote oppervlakken. Meer onderzoek is vereist om de lengtelimieten van beide patroneringstechnieken te vinden. In een directe vergelijking is het Pd-gekatalyseerd afzetten van koper minder goed te controleren, hetgeen tot onregelmatige vormen en variabele hoogtes leidt. Het eenvoudig patroneren van dunne maar zeer geleidende zilverdraden uit langdurig stabiele, waterige oplossingen zoals beschreven in hoofdstuk 7, laat de integratie in een R2R-lijn toe. Een mogelijke oplossingsgebaseerde route zou dus denkbaar zijn, waarin alle in dit proefschrift onderzochte patroneringstechnieken geïntegreerd worden in een goedkoop, grootschalig fabricageproces voor het maken van flexibele elektronica. Met UV NIL zou een driedimensionale plattegrond van het device kunnen worden gedefinieerd, met in zijn topografie of ontwerp aanwijzingen die de metaalprecursors (of polymeren) hun plaats wijzen, om zo de individuele componenten van de flexibele elektronica te vormen. Zulke fabricagemethoden zullen de strategieën zijn voor toekomstige generaties van flexibele elektronica.

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# Curriculum Vitae

Pieter Frederik Moonen was born on February 29th, 1984 in Leiden (The Netherlands). After graduating from the European School in Munich (Germany) in 2002, he went to study chemistry at the University of Cologne (Germany). He received his Master of Science degree (*Diplom Chemiker*) in Chemistry in January 2008, working in the field of physical chemistry on "Microcontact Printing in Sensors and their Analysis with Surface-Plasmon-Resonance Ellipsometry" under supervision of Prof. Klaus Meerholz.

In the beginning of 2008 he started as a PhD candidate at the University of Twente in the Molecular Nanofabrication group of Prof. Jurriaan Huskens. His research focused mainly on nanoimprint lithography-based patterning strategies of flexible electronics. The work was performed in close collaboration with the Holst Centre / TNO in Eindhoven. The results of his research are described in this thesis.